IMU-3000
Motion Processing Unit
Product Specification
Rev 1.0

CONTENTS

1 Document Information

1.1 Revision History

Revision Date	Revision	Description
05/26/2010	1.0	Initial Release

1.2 Purpose and Scope

This document is a preliminary product specification, providing a description, specifications, and design related information for the IMU-3000™ Motion Processing Unit™. The IMU-3000 MPL Functional Specification describes in detail the API and System Layer routines needed for interfacing to the IMU-3000.

Electrical characteristics are based upon simulation results and limited characterization data of advanced samples only. Specifications are subject to change without notice. Final specifications will be updated based upon characterization of final silicon.

1.3 Product Overview

The IMU-3000 Motion Processing Unit (IMU™) is the world's first IMU solution with 6-axis sensor fusion for consumer applications. The IMU-3000 has an embedded 3-axis gyroscope and Digital Motion Processor™ (DMP™) hardware accelerator engine with a secondary I^2C port that interfaces to third party digital accelerometers to deliver a complete 6-axis sensor fusion output to its primary I^2C port. This combines both linear and rotational motion into a single data stream for the application. The device is ideally suited for a wide variety of consumer products requiring a rugged, low-cost motion processing solution for applications in game controllers, remote controls for broadband connected TVs and set top boxes, sports, fitness, medical and other applications. By providing an integrated sensor fusion output, the IMU-3000 offloads the intensive motion processing computation requirements from the host processor, reducing the need for frequent polling of the motion sensor output and enabling use of low cost, low power microcontrollers.

The IMU-3000 features a 3-axis digital gyro with programmable full-scale ranges of ±250, ±500, ±1000, and ±2000 degrees/sec (dps), which is useful for precision tracking of both fast and slow motions. Rate noise performance sets the industry standard at 0.02 dps/√Hz, providing the highest-quality user experience in pointing and gaming applications. Factory-calibrated initial sensitivity reduces production-line calibration requirements. The part's on-chip FIFO and dedicated I^2C-master accelerometer sensor bus simplify system timing and lower system power consumption; the sensor bus allows the IMU-3000 to directly acquire data from the off-chip accelerometer without intervention from an external processor, while the FIFO allows a system microcontrollers to burst read the sensor data and then go to sleep while the IMU collects more data. Other industry-leading features include on-chip16-bit ADCs, programmable digital filters, a precision clock with 1% variation from -40°C to 85°C, an embedded temperature sensor, programmable interrupts, and a low 13mW power consumption. Parts are available with an I^2C serial interface, a VDD operating range of 2.1 to 3.6V, and a VLOGIC interface voltage from 1.71V to 3.6V.

By leveraging its patented and volume-proven Nasiri-Fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the IMU-3000 package size down to a revolutionary footprint of 4x4x0.9mm (QFN), while providing the highest performance, lowest noise, and the lowest cost semiconductor packaging to address a wide range of handheld consumer electronic devices. The device provides the highest robustness by supporting 10,000*g* shock in operation. The highest cross-axis isolation is achieved by design from its single silicon integration.

The IMU-3000 was designed to connect directly with a third-party 3-axis digital accelerometer, which slaves directly to the IMU-3000 master and can be clocked from the internal phase locked loop of the IMU-3000 device, providing highly accurate timing for a true 6-axis motion processing solution previously only available in costly and bulky inertial measurement units.

1.4 Applications

- Game controllers
- 3D Remote controls for Internet connected TVs and Set Top Boxes
- Health and sports monitoring
- Motion tracking
- Gesture recognition and advanced user interfaces

2 Features

The IMU-3000 Motion Processing Unit includes a wide range of features:

2.1 Sensors

- X-, Y-, Z-Axis angular rate sensors (gyros) on one integrated circuit
- Digital-output temperature sensor
- 6-axis motion processing capability using secondary I^2C interface to directly connect to a digital 3-axis third-party accelerometer
- Factory-calibrated scale factor
- High cross-axis isolation via proprietary MEMS design
- 10,000*g* shock tolerant

2.2 Digital Output

- Fast Mode (400kHz) I^2C serial interface
- 16-bit ADCs for digitizing sensor outputs
- Angular rate sensors (gyros) with applications-programmable full-scale-range of ±250°/sec, ±500°/sec, ±1000°/sec, or ±2000°/sec.

2.3 Motion Processing

- Embedded Digital Motion Processing™ (DMP™) engine supports 3D motion processing. When used together with a digital 3-axis third party accelerometer, the IMU-3000 collects the accelerometer data via a dedicated interface, while synchronizing data sampling at a user defined rate. The total data set obtained by the IMU-3000 includes 3-axis gyroscope data, 3-axis accelerometer data, and temperature data.
- FIFO buffers complete data set, reducing timing requirements on the system processor and saving power by letting the processor burst read the FIFO data, and then go into a low-power sleep mode while the IMU collects more data.
- Data collection polled or interrupt driven with on-chip programmable interrupt functionality
- Programmable low-pass filters

2.4 Clocking

- On-chip timing generator clock frequency ±1% variation over full temperature range
- Optional external clock inputs of 32.768kHz or 19.2MHz
- 1MHz clock output to synchronize with digital 3-axis accelerometer

2.5 Power

- VDD analog supply voltage range of 2.1V to 3.6V
- Flexible VLOGIC reference voltage allows for I^2C interface voltages from 1.71V to VDD
- Power consumption with all three axis active: 6.5mA
- Sleep mode: 5µA
- Each axis can be individually powered down

2.6 Package

- 4x4x0.9mm QFN plastic package
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 Electrical Characteristics

3.1 Sensor Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 2.5V, T_A=25°C.

Parameter	Conditions	Min	Typical	Max	Unit	Notes
GYRO SENSITIVITY						
Full-Scale Range	FS_SEL=0		±250		º/s	4
	FS_SEL=1		±500			4
	FS_SEL=2		±1000			4
	FS_SEL=3		±2000			4
Gyro ADC Word Length			16		Bits	3
Sensitivity Scale Factor	FS_SEL=0		131		LSB/(º/s)	1
	FS_SEL=1		65.5			3
	FS_SEL=2		32.8			3
	FS_SEL=3		16.4			3
Sensitivity Scale Factor Tolerance	25°C	-3		+3	%	2
Sensitivity Scale Factor Variation Over Temperature			±2		%	2
Nonlinearity	Best fit straight line; 25°C		0.2		%	6
Cross-Axis Sensitivity			2		%	6
GYRO ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±40		º/s	2
ZRO Variation Over Temperature	-40°C to +85°C		±30		º/s	2
Power-Supply Sensitivity (1-10Hz)	Sine wave, 100mVpp; VDD=2.2V		0.2		º/s	5
Power-Supply Sensitivity (10 - 250Hz)	Sine wave, 100mVpp; VDD=2.2V		0.2		º/s	5
Power-Supply Sensitivity (250Hz - 100kHz)	Sine wave, 100mVpp; VDD=2.2V		4		º/s	5
Linear Acceleration Sensitivity	Static		0.1		º/s/*g*	6
GYRO NOISE PERFORMANCE	**FS_SEL=0**					
Total RMS Noise	DLPFCFG=2 (100Hz)		0.2		º/s-rms	1
Rate Noise Spectral Density	At 10Hz		0.02		º/s/√Hz	2
GYRO START-UP TIME	**DLPFCFG=0**					
ZRO Settling	to ±1º/s of Final		50		ms	5
TEMPERATURE SENSOR						
Range			-40 to 85		ºC	2
Sensitivity	Untrimmed		280		LSB/ºC	2
Room-Temperature Offset	35°C		-7200		LSB	1
Absolute Accuracy	35°C		TBD		°C	
Linearity	Best fit straight line (-30°C to +85°C)		±1		°C	2
TEMPERATURE RANGE						
Specified Temperature Range		-40		85	ºC	2

Notes:

1. Tested in production
2. Based on characterization of 30 parts over temperature on evaluation board or in socket
3. Based on design, through modeling and simulation across PVT
4. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
5. Based on characterization of 5 parts over temperature
6. Tested on 5 parts at room temperature

3.2 Electrical Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5V, T_A = 25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
VDD POWER SUPPLY						
Operating Voltage Range		2.1		3.6	V	2
Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value (see Figure in Section 4.4)	0		5	ms	2
Normal Operating Current			6.5		mA	1
Sleep Mode Current			5		µA	5
VLOGIC REFERENCE VOLTAGE						
Voltage Range	VLOGIC must be ≤VDD at all times	1.71		VDD	V	
Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value (see Figure in Section 4.4)			1	ms	6
Normal Operating Current			100		µA	
START-UP TIME FOR REGISTER READ/WRITE			20	100	ms	5
I^2C ADDRESS						
	AD0 = 0		1101000			6
	AD0 = 1		1101001			6
DIGITAL INPUTS (AD0, CLKIN)						
V_{IH}, High Level Input Voltage		0.7*VDD			V	5
V_{IL}, Low Level Input Voltage				0.3*VDD	V	5
C_I, Input Capacitance				5	pF	7
DIGITAL OUTPUT (INT)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ	0.9*VLOGIC			V	2
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1MΩ			0.1*VLOGIC	V	2
$V_{OL.INT1}$, INT Low-Level Output Voltage	OPEN=1, 0.3mA sink current			0.1	V	2
Output Leakage Current	OPEN=1		100		nA	4
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	4

Notes:

1. Tested in production
2. Based on characterization of 30 parts over temperature on evaluation board or in socket
4. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
5. Based on characterization of 5 parts over temperature
6. Refer to Section 4.4 for the recommended power-on procedure
7. Guaranteed by design

3.3 Electrical Specifications, continued

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 2.5V, T_A=25°C.

Parameters	Conditions	Typical	Units	Notes
Primary I^2C I/O (SCL, SDA)				
V_{IL}, LOW-Level Input Voltage		-0.5V to 0.3*VLOGIC	V	2
V_{IH}, HIGH-Level Input Voltage		0.7*VLOGIC to VLOGIC + 0.5V	V	2
V_{hys}, Hysteresis		0.1*VLOGIC	V	2
V_{OL1}, LOW-Level Output Voltage	3mA sink current	0 to 0.4	V	2
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V	3	mA	2
	V_{OL} = 0.6V	5	mA	2
Output Leakage Current		100	nA	4
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	Cb bus capacitance in pF	20+0.1Cb to 250	ns	2
C_I, Capacitance for Each I/O pin		10	pF	5
Secondary I^2C I/O (AUX_CL, AUX_DA)	**AUX_VDDIO=0**			
V_{IL}, LOW-Level Input Voltage		-0.5V to 0.3*VLOGIC	V	2
V_{IH}, HIGH-Level Input Voltage		0.7*VLOGIC to VLOGIC+0.5V	V	2
V_{hys}, Hysteresis		0.1*VLOGIC	V	2
V_{OL1}, LOW-Level Output Voltage	VLOGIC > 2V; 1mA sink current	0 to 0.4	V	2
V_{OL3}, LOW-Level Output Voltage	VLOGIC < 2V; 1mA sink current	0 to 0.2*VLOGIC	V	2
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V	1	mA	2
	V_{OL} = 0.6V	1	mA	2
Output Leakage Current		100	nA	4
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	Cb bus capacitance in pF	20+0.1Cb to 250	ns	2
C_I, Capacitance for Each I/O pin		10	pF	5
Secondary I^2C I/O (AUX_CL, AUX_DA)	**AUX_VDDIO=1**			
V_{IL}, LOW-Level Input Voltage		-0.5 to 0.3*VDD	V	2
V_{IH}, HIGH-Level Input Voltage		0.7*VDD to VDD+0.5V	V	2
V_{hys}, Hysteresis		0.1*VDD	V	2
V_{OL1}, LOW-Level Output Voltage	1mA sink current	0 to 0.4	V	2
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V	1	mA	2
	V_{OL} = 0.6V	1	mA	2
Output Leakage Current		100	nA	4
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	Cb bus capacitance in pF	20+0.1Cb to 250	ns	2
C_I, Capacitance for Each I/O pin		10	pF	5

Notes:

2. Based on characterization of 5 parts over temperature.
4. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
5. Guaranteed by design

3.4 Electrical Specifications, continued

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 2.5V, T_A=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
INTERNAL CLOCK SOURCE	**CLKSEL=0,1,2,3**					
Sample Rate, Fast	DLPFCFG=0 SAMPLERATEDIV = 0		8		kHz	4
Sample Rate, Slow	DLPFCFG=1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1		kHz	4
Reference Clock Output	CLKOUTEN = 1		1.024		MHz	4
Clock Frequency Initial Tolerance	CLKSEL=0, 25°C	-3		+3	%	1
	CLKSEL=1,2,3; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLKSEL=0		-15 to +10		%	2
	CLKSEL=1,2,3		±1		%	2
PLL Settling Time	CLKSEL=1,2,3		1		ms	3
EXTERNAL 32.768kHz CLOCK	**CLKSEL=4**					
External Clock Frequency			32.768		kHz	3
External Clock Jitter	Cycle-to-cycle rms		1 to 2		µs	3
Sample Rate, Fast	DLPFCFG=0 SAMPLERATEDIV = 0		8.192		kHz	3
Sample Rate, Slow	DLPFCFG=1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1.024		kHz	3
Reference Clock Output	CLKOUTEN = 1		1.0486		MHz	3
PLL Settling Time			1		ms	3
EXTERNAL 19.2MHz CLOCK	**CLKSEL=5**					
External Clock Frequency			19.2		MHz	3
Sample Rate, Fast	DLPFCFG=0 SAMPLERATEDIV = 0		8		kHz	3
Sample Rate, Slow	DLPFCFG=1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1		kHz	3
Reference Clock Output	CLKOUTEN = 1		1.024		MHz	3
PLL Settling Time			1		ms	3

Notes:

1. Tested in production
2. Based on characterization of 30 parts over temperature on evaluation board or in socket
3. Based on design, through modeling and simulation across PVT
4. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
5. Based on characterization of 5 parts over temperature.

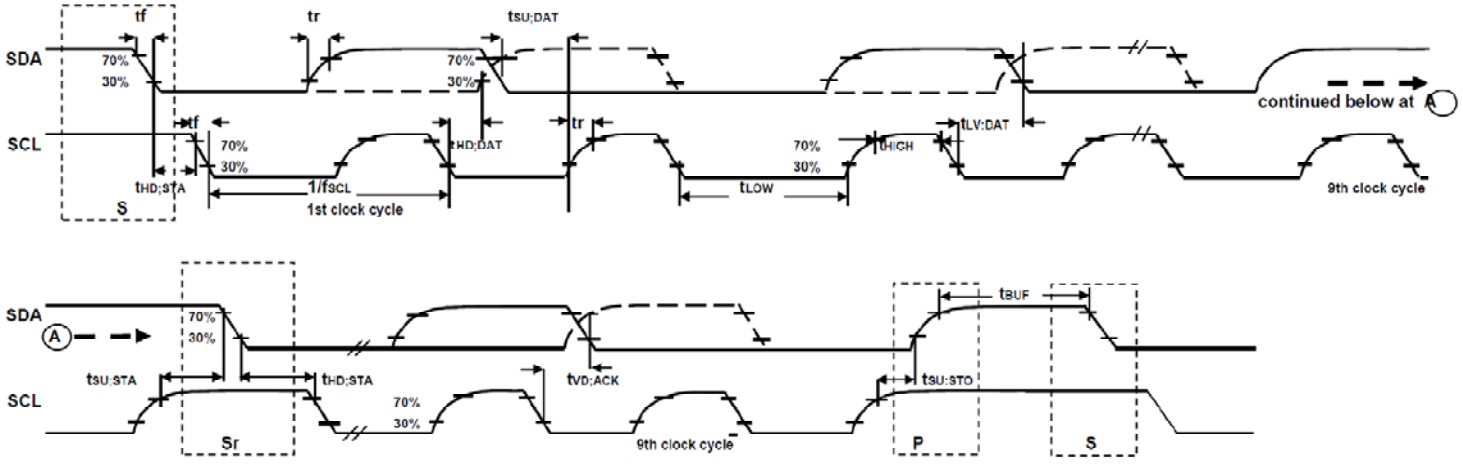
3.5 I²C Timing Characterization

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 1.8V±5%, 2.5V±5%, 3.0V±5%, or 3.3V±5%, T_A=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency		0		400	kHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	1
t_{LOW}, SCL Low Period		1.3			µs	1
t_{HIGH}, SCL High Period		0.6			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1
t_r, SDA and SCL Rise Time	Cb bus cap. from 10 to 400pF	20+0.1 Cb		300	ns	1
t_f, SDA and SCL Fall Time	Cb bus cap. from 10 to 400pF	20+0.1 Cb		300	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	1
C_b, Capacitive Load for each Bus Line				400	pF	2
$t_{VD.DAT}$, Data Valid Time				0.9	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	1

Notes:

1. Based on characterization of 5 parts over temperature on evaluation board or in socket
2. Guaranteed by design



I²C Bus Timing Diagram

3.6 Absolute Maximum Ratings

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

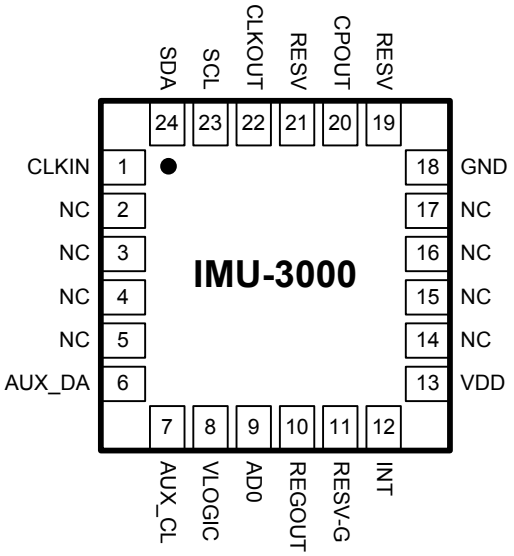
Absolute Maximum Ratings

Parameter	Rating
Supply Voltage, VDD	-0.5V to +6V
VLOGIC Input Voltage Level	-0.5V to VDD + 0.5V
REGOUT	-0.5V to 2V
Input Voltage Level (CLKIN, AUX_DA, AD0, INT, SCL, SDA)	-0.5V to VDD + 0.5V
CPOUT (2.1V ≤ VDD ≤ 3.6V)	-0.5V to 30V
Acceleration (Any Axis, unpowered)	10,000*g* for 0.3ms
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	1.5kV (HBM); 200V (MM)

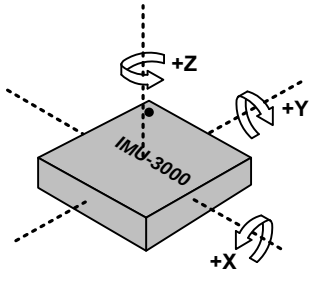
4 Applications Information

4.1 Pin Out and Signal Description

Pin Number	Pin Name	Pin Description
1	CLKIN	External reference clock input
6	AUX_DA	Interface to a 3rd party accelerometer, SDA pin. Logic levels are set to be either VDD or VLOGIC. See Section 7 for more details.
7	AUX_CL	Interface to a 3rd party accelerometer, SCL pin. Logic levels are set to be either VDD or VLOGIC. See Section 7 for more details.
8	VLOGIC	Digital I/O supply voltage. VLOGIC must be ≤ VDD at all times.
9	AD0	I^2C Slave Address LSB
10	REGOUT	Regulator filter capacitor connection
11	RESV-G	Reserved – Connect to Ground.
12	INT	Interrupt digital output (totem pole or open-drain)
13	VDD	Power supply voltage and Digital I/O supply voltage
18	GND	Power supply ground
19	RESV	Reserved. Do not connect.
20	CPOUT	Charge pump capacitor connection
21	RESV	Reserved. Do not connect.
22	CLKOUT	1MHz clock output for third-party accelerometer synchronization
23	SCL	I^2C serial clock
24	SDA	I^2C serial data
2, 3, 4, 5, 14, 15, 16, 17	NC	Not internally connected. May be used for PCB trace routing.

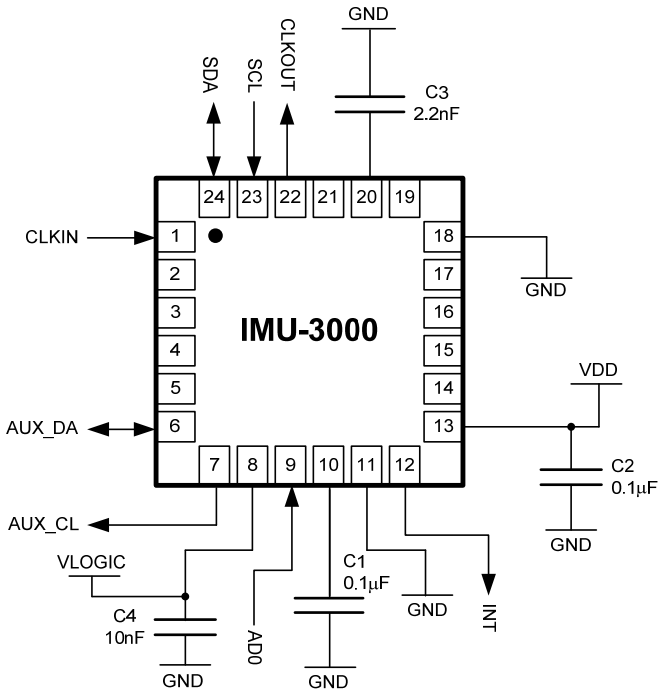


QFN Package (Top View)
24-pin, 4mm x 4mm x 0.9mm



Orientation of Axes of Sensitivity and Polarity of Rotation

4.2 Typical Operating Circuit

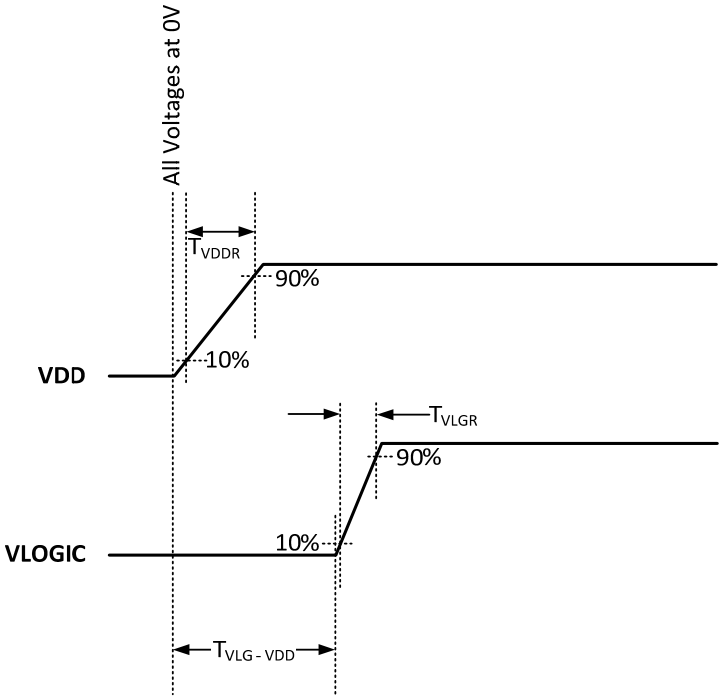


Typical Operating Circuit

4.3 Bill of Materials for External Components

Component	Label	Specification	Quantity
VDD Bypass Capacitor	C1	Ceramic, X7R, 0.1µF ±10%, 4V	1
Regulator Filter Capacitor	C2	Ceramic, X7R, 0.1µF ±10%, 2V	1
Charge Pump Capacitor	C3	Ceramic, X7R, 2.2nF ±10%, 50V	1
VLOGIC Bypass Capacitor	C4	Ceramic, X7R, 10nF ±10%, 4V	1

4.4 Recommended Power-on Procedure

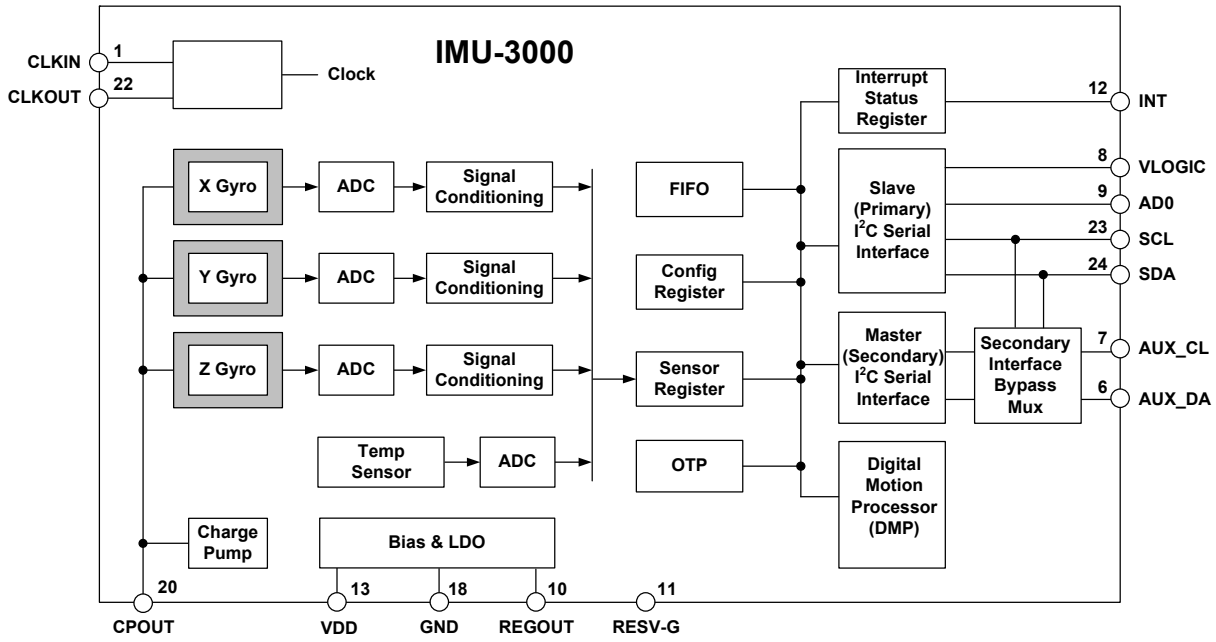


Power-Up Sequencing

1. T_{VDDR} is VDD rise time: Time for VDD to rise from 10% to 90% of its final value
2. T_{VDDR} is ≤10msec
3. T_{VLGR} is VLOGIC rise time: Time for VLOGIC to rise from 10% to 90% of its final value
4. T_{VLGR} is ≤1msec
5. $T_{VLG-VDD}$ is the delay from the start of VDD ramp to the start of VLOGIC rise
6. $T_{VLG-VDD}$ is 0 to 20msec but VLOGIC amplitude must always be ≤VDD amplitude
7. VDD and VLOGIC must be monotonic ramps

5 Functional Overview

5.1 Block Diagram



5.2 Overview

The IMU-3000 is comprised of the following key blocks / functions:

- Three-axis MEMS rate gyroscope sensors with 16-bit ADCs and signal conditioning
- Digital Motion Processor (DMP)
- Primary I^2C serial communications interface
- Secondary I^2C serial interface for 3rd party accelerometer
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDO
- Charge Pump

5.3 Three-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning

The IMU-3000 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X, Y, and Z axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps). ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

5.4 Digital Motion Processor

The embedded Digital Motion Processor (DMP) is located within the IMU-3000 and offloads computation of motion processing algorithms from the host processor. The DMP acquires and processes data from the on-

chip gyroscopes and an external accelerometer. The resulting data can be read from IMU-3000's FIFO. The DMP has access to certain of the IMU's external pins, which can be used for synchronizing external devices to the motion sensors, or generating interrupts for the application.

The purpose of the DMP is to offload both timing requirements and processing power from the host processor. Typically, motion processing algorithms should be run at a high rate, often around 200Hz, in order to provide accurate results with low latency. This is required even if the application updates at a much lower rate; for example, a low power user interface may update as slowly as 5Hz, but the motion processing should still run at 200Hz. The DMP can be used as a tool in order to minimize power, simplify timing and software architecture, and save valuable MIPS on the host processor for use in the application.

5.5 Primary I^2C Serial Communications Interface

The IMU-3000 communicates to a system processor using the I^2C serial interface; the device always acts as a slave when communicating to the system processor. **The logic level for communications to the master is set by the voltage on the VLOGIC pin.** The LSB of the of the I^2C slave address is set by pin 9 (AD0).

5.6 Secondary I^2C Serial Interface for third-party Accelerometer

The IMU-3000 has a secondary I^2C bus for communicating to an off-chip 3-axis digital output accelerometer. This bus has two operating modes: I^2C Master Mode, where the IMU-3000 acts as a master to an external accelerometer connected to the secondary I^2C bus; and Pass-Through Mode, where the IMU-3000 directly connects the primary and secondary I^2C buses together, to allow the system processor to directly communicate with the external accelerometer.

Secondary I^2C Bus Modes of Operation:

- I^2C Master Mode: allows the IMU-3000 to directly access the data registers of an external digital accelerometer. In this mode, the IMU-3000 directly obtains sensor data from an accelerometer thus allowing the on-chip DMP to generate sensor fusion data without intervention from the system applications processor. In I^2C master mode, the IMU-3000 can be configured to perform burst reads, returning the following data from the accelerometer:
    - X accelerometer data (2 bytes)
    - Y accelerometer data (2 bytes)
    - Z accelerometer data (2 bytes)
- Pass-Through Mode: allows an external system processor to act as master and directly communicate to the external accelerometer connected to the secondary I^2C bus pins (AUX_DA and AUX_CL). This is useful for configuring the accelerometer, or for keeping the IMU-3000 in a low-power mode, when only the accelerometer is to be used. In this mode, the secondary I^2C bus control logic (third-party accelerometer Interface block) of the IMU-3000 is disabled, and the secondary I^2C pins AUX_DA and AUX_CL (Pins 6 and 7) are connected to the main I^2C bus (Pins 23 and 24) through analog switches.

Secondary I^2C Bus I/O Logic Levels

The logic levels of the secondary I^2C bus can be programmed to be either VDD or VLOGIC (see Sections 7 and 8).

6 Clocking

6.1 Internal Clock Generation

The IMU-3000 has a flexible clocking scheme, allowing for a variety of internal or external clock sources for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, the DMP, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

- An internal relaxation oscillator
- Any of the X, Y, or Z gyros (MEMS oscillators with a variation of ±1% over temperature range)

Allowable external clocking sources are:

- 32.768kHz square wave
- 19.2MHz square wave

Which source to select for generating the internal synchronous clock depends on the availability of external sources and the requirements for power consumption and clock accuracy. Most likely, these requirements will vary by mode of operation. For example, in one mode, where the biggest concern is power consumption, one may wish to operate the Digital Motion Processor of the IMU-3000 to process accelerometer data, while keeping the gyros off. In this case, the internal relaxation oscillator is a good clock choice. However, in another mode, where the gyros are active, selecting the gyros as the clock source provides for a more-accurate clock source.

Clock accuracy is important, since timing errors directly affect the distance and angle calculations performed by the Digital Motion Processor (or by extension, by any processor).

There are also start-up conditions to consider. When the IMU-3000 first starts up, the device operates off of its internal clock, until programmed to operate from another source. This allows the user, for example, to wait for the MEMS oscillators to stabilize before they are selected as the clock source.

6.2 Clock Output

In addition, the IMU-3000 provides a 1MHz clock output, which allows the device to operate synchronously with an external digital 3-axis accelerometer. Operating synchronously provides for higher-quality sensor fusion data, since the sampling instant for the sensor data can be set to be coincident for all sensors.

6.3 Sensor Data Registers

The sensor data registers contain the latest gyro and temperature data. They are read-only registers, and are accessed via the Serial Interface. Data from these registers may be read anytime, however, the interrupt function may be used to determine when new data is available.

6.4 FIFO

The IMU-3000 contains a 512-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines what data goes into it, with possible choices being gyro data, accelerometer data, temperature readings, and auxiliary ADC readings. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

6.5 Interrupts

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) Digital Motion Processor Done (programmable function); (3) new data is available to be read (from the FIFO and Data registers); and (4) the IMU-3000 did not receive an acknowledge from the accelerometer on the Secondary I^2C bus. The interrupt status can be read from the Interrupt Status register.

6.6 Digital-Output Temperature Sensor

An on-chip temperature sensor and ADC are used to measure the IMU-3000 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

6.7 Bias and LDO

The bias and LDO section generates the internal supply and the reference voltages and currents required by the IMU-3000. Its inputs are an unregulated VDD of 2.1V to 3.6V and a VLOGIC - logic reference supply voltage - of 1.71V to VDD. The LDO output is bypassed by a 0.1µF capacitor at REGOUT.

6.8 Charge Pump

An on-board charge pump generates the high voltage required for the MEMS oscillators. Its output is bypassed by a 2.2nF capacitor at CPOUT.

7 Digital Interface

7.1 I²C Serial Interface

The internal registers of the IMU-3000 can be accessed using I²C at up to 400kHz.

Serial Interface

Pin Number	Pin Name	Pin Description
8	VLOGIC	Digital I/O supply voltage. VLOGIC must be ≤ VDD at all times.
9	AD0	I²C Slave Address LSB
23	SCL	I²C serial clock
24	SDA	I²C serial data

7.1.1 I²C Interface

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The IMU-3000 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400kHz.

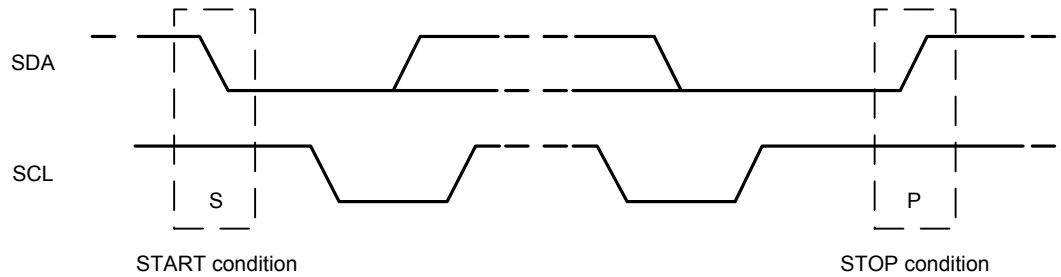
The slave address of the IMU-3000 is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin ADO. This allows two IMU-3000s to be connected to the same I²C bus. When used in this configuration, the address of the one of the devices should be b1101000 (pin ADO is logic low) and the address of the other should be b1101001 (pin AD0 is logic high). The I²C address is stored in the WHO_AM_I register.

I²C Communications Protocol

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

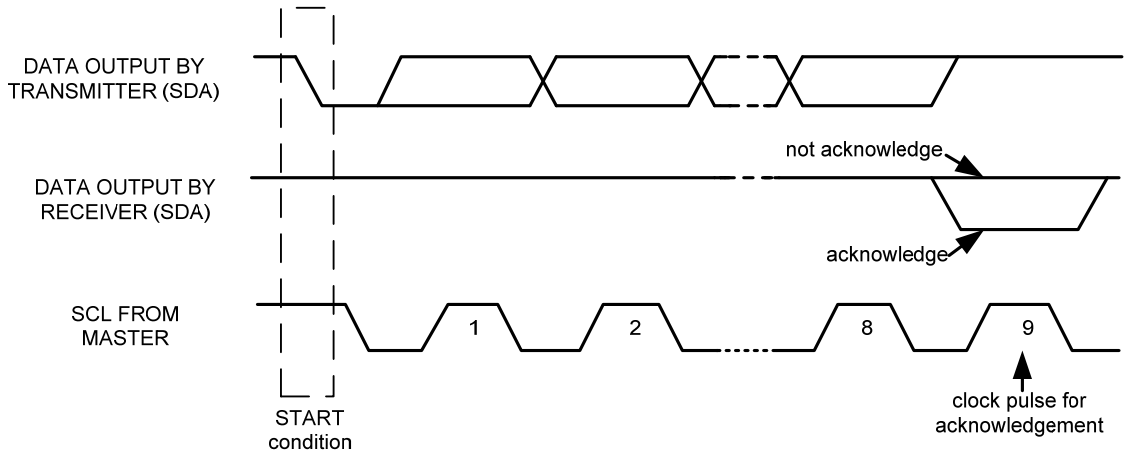


START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8 bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

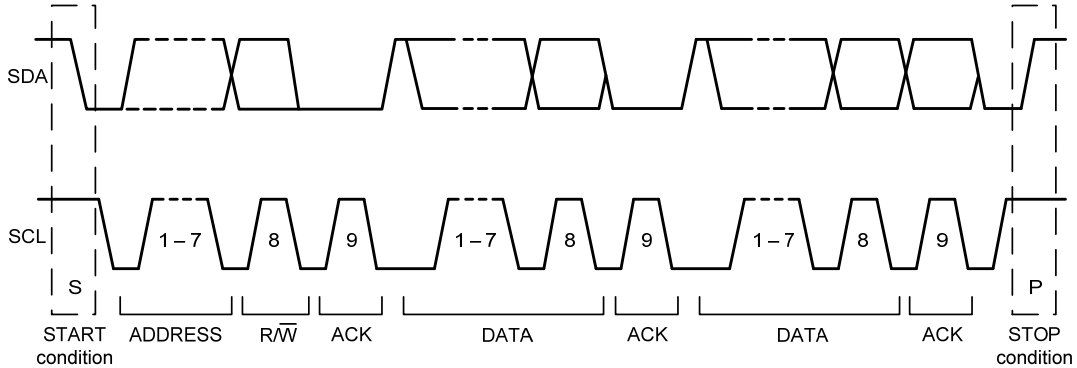
If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).



Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.



Complete I²C Data Transfer

To write the internal IMU-3000 registers, the master transmits the start condition (S), followed by the I^2C address and the write bit (0). At the 9th clock cycle (when the clock is high), the IMU-3000 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the IMU-3000 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the IMU-3000 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal IMU-3000 registers, the master sends a start condition, followed by the I^2C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the IMU-3000, the master transmits a start signal followed by the slave address and read bit. As a result, the IMU-3000 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

I^2C Terms

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I^2C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	IMU-3000 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Serial Interface Considerations

7.2 Supported Interfaces

The IMU-3000 supports I^2C communications on both its primary (microprocessor) serial interface and its secondary (accelerometer) interface.

7.3 Logic Levels

The IMU-3000 accelerometer bus I/O logic levels are set to be either VDD or VLOGIC, as shown in the table below.

I/O Logic Levels vs. *AUX_VDDIO bit*

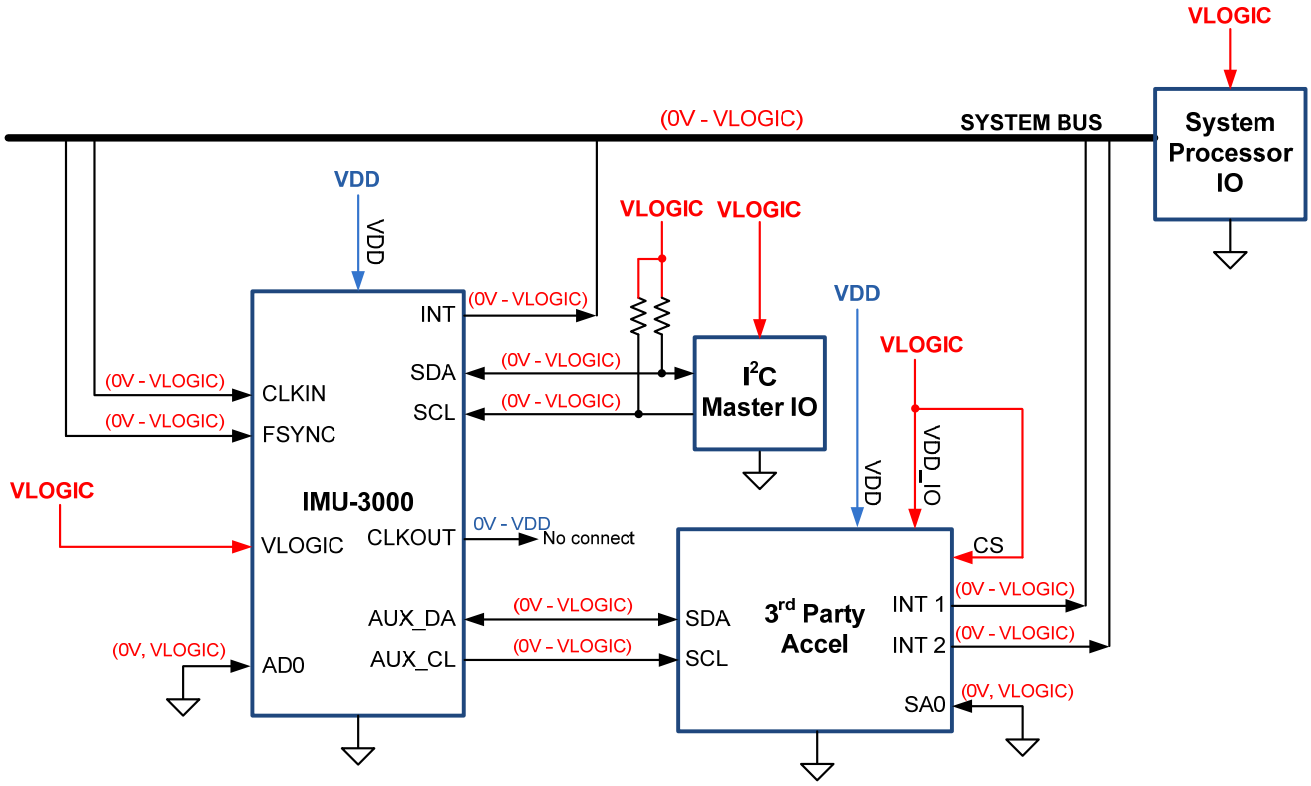
AUX_VDDIO	MICROPROCESSOR LOGIC LEVELS (Pins: SDA, SCL, AD0, CLKIN, INT)	ACCELEROMETER LOGIC LEVELS (Pins: AUX_DA, AUX_CL)
0	VLOGIC	VLOGIC
1	VLOGIC	VDD

Notes:
1. CLKOUT has logic levels that are always referenced to VDD
2. The power-on-reset value for *AUX_VDDIO* is 0.

VLOGIC may be set to be equal to VDD or to another voltage, such that at all times VLOGIC is ≤ VDD. When *AUX_VDDIO* is set to 0 (its power-on-reset value), VLOGIC is the reference voltage for both the microprocessor system bus and the accelerometer secondary bus, as shown in the figure of Section 8.2.1. When *AUX_VDDIO* is set to 1, VLOGIC is the reference voltage for the microprocessor system bus and VDD is the reference voltage for the accelerometer secondary bus, as shown in the figure of Section 8.2.2.

7.3.1 *AUX_VDDIO* = 0

The figure below shows logic levels and voltage connections for AUX_VDDIO = 0. Note that the actual configuration will depend on the type of third-party accelerometer used.



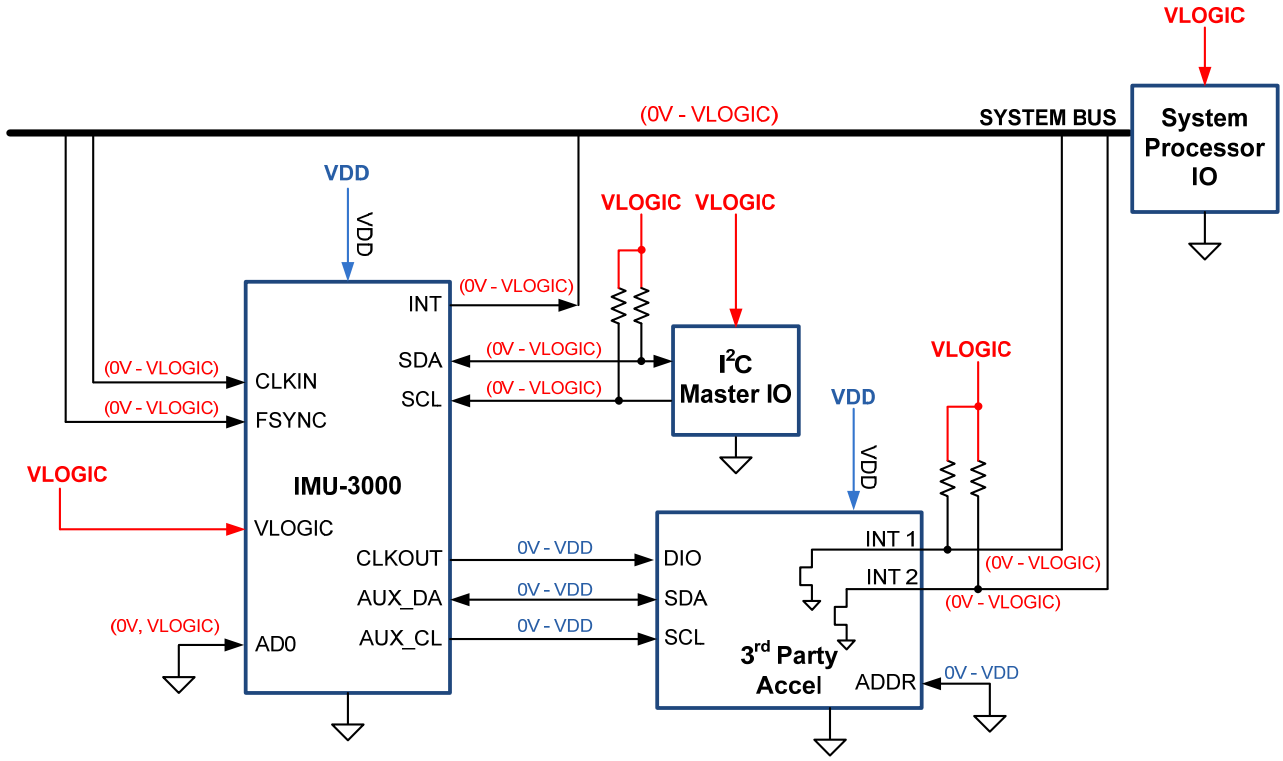
Notes:

1. The AUX_*VDDIO* register bit determines the I/O voltage levels of AUX_DA and AUX_CL (0 = set output levels relative to VLOGIC)
2. CLKOUT is always referenced to VDD
3. Other IMU-3000 logic I/O are always referenced to VLOGIC

I/O Levels and Connections for *AUX_VDDIO* = 0

7.3.2 *AUX_VDDIO* = 1

When *AUX_VDDIO* is set to 1 by the user, VLOGIC is the reference voltage for the microprocessor system bus and VDD is the reference voltage for the accelerometer secondary bus, as shown in the figure below. This is useful when interfacing to a third-party accelerometer where there is only one supply for both the logic and analog sections of the 3rd party accelerometer.



Voltage/ Configuration	Configuration 1	Configuration 2
VLOGIC	1.8V±5%	3.0V±5%
VDD	2.5V±5%	3.0V±5%
AUX_VDDIO	1	1

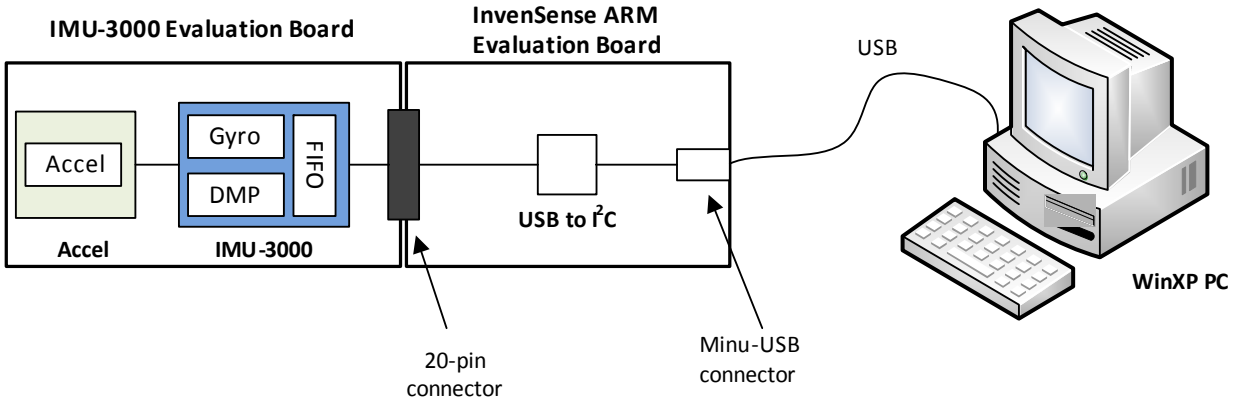
Notes:

1. The *AUX_VDDIO* register bit determines the I/O voltage levels of AUX_DA and AUX_CL (1 = set output levels relative to VDD)
2. CLKOUT is always referenced to VDD
3. Other IMU-3000 logic I/O are always referenced to VLOGIC
4. If third-party accelerometer logic levels are referenced to VDD; setting INT1 and INT2 to open-drain configuration provides voltage compatibility when VDD ≠ VLOGIC.
   When VDD = VLOGIC, INT1 and INT2 may be set to push-pull outputs, and the external pull-up resistors will not be needed.

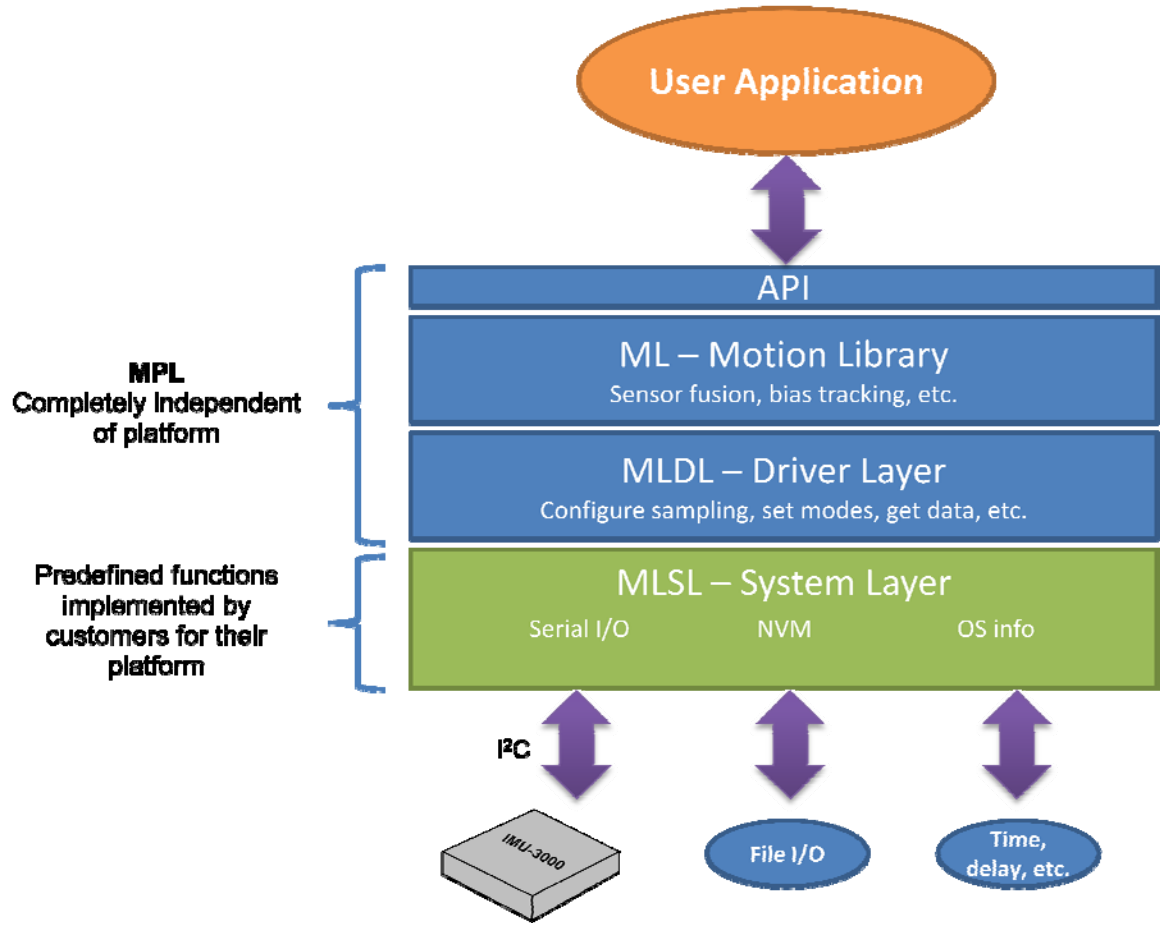
I/O Levels and Connections for Two Example Power Configurations (*AUX_VDDIO* = 1)

8 Motion Processing Library (MPL)

To assist in the rapid development and deployment of products using the IMU-3000, InvenSense provides a Motion Processing Library (MPL) software development kit that has been verified to work in the hardware and software environment shown in the figure below.



The MPL contains the core algorithm engines for motion processing, and includes an API layer which provides a simple interface into using these engines (see figure below).



The MPL communicates with the System Layer, which is a platform-specific interface into the hardware and software environment; this System Layer software must be implemented by the customer for his particular environment. The software development kit includes shell functions to speed up the development of this System Layer software. The MPL is independent of the Operating System (OS) since the System Layer software handles OS-specific requirements.

The purpose of the DMP is to offload both timing requirements and processing requirements from the host processor. Typically, raw data integration (sensor fusion) should be run at a high rate, often around 200Hz, in order to provide accurate results with low latency. This is required even if the application updates at a much lower rate; for example, a low power user interface may update as slowly as 5Hz, but the sensor fusion should still run at 200Hz. The DMP can be used to minimize power, simplify timing and software architecture, and saving valuable MIPS on the host processor for use in the application.

The IMU-3000 MPL Functional Specification describes in detail the API and System Layer routines needed for interfacing to the IMU-3000.

8.1 Demo Software

InvenSense provides demonstration software in the form of source code and a compiled demonstration that runs on a PC running Windows XP. This software works in conjunction with the hardware shown in the figure at the top of Section 8. The PC demo software provides the functionality that allows a user to become familiar with the use of gyros and accelerometers.

9 Register Map

Addr (Hex)	Addr (Decimal)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	WHO_AM_I	R/W	0	ID						-
C	12	X_OFFS_USRH	R/W	X_OFF_H							
D	13	X_OFFS_USRL	R/W	X_OFF_L							
E	14	Y_OFFS_USRH	R/W	Y_OFFS_H							
F	15	Y_OFFS_USRL	R/W	Y_OFFS_L							
10	16	Z_OFFS_USRH	R/W	Z_OFFS_H							
11	17	Z_OFFS_USRL	R/W	Z_OFFS_L]							
12	18	FIFO_EN	R/W	TEMP_OUT	GYRO_XOUT	GYRO_YOUT	GYRO_ZOUT	AUX_XOUT	AUX_YOUT	AUX_ZOUT	FIFO_FOOTER
13	19	AUX_VDDIO	R/W	0	0	0	0	0	AUX_VDDIO	0	0
14	20	AUX_SLV_ADDR	R/W	CLKOUT EN	AUX_ID						
15	21	SMPLRT_DIV	R/W	SMPLRT_DIV							
16	22	DLPF_FS	R/W	0	0	0	FS_SEL		DLPF_CFG		
17	23	INT_CFG	R/W	ACTL	OPEN	LATCH_INT_EN	INT_ANYRD_2CLEAR	I2C_MST_ERR_EN	IMU_RDY_EN	DMP_DONE_EN	RAW_RDY_ EN
18	24	AUX_BURST_ADDR	R/W	BURST_ADDR							
1A	26	INT_STATUS	R	FIFO_FULL	-	-		I2C_MST_ERR	IMU_RDY	DMP_DONE	RAW_DATA_RDY
1B	27	TEMP_OUT_H	R	TEMP_OUT_H							
1C	28	TEMP_OUT_L	R	TEMP_OUT_L							
1D	29	GYRO_XOUT_H	R	GYRO_XOUT_H							
1E	30	GYRO_XOUT_L	R	GYRO_XOUT_L							
1F	31	GYRO_YOUT_H	R	GYRO_YOUT_H							
20	32	GYRO_YOUT_L	R	GYRO_YOUT_L							
21	33	GYRO_ZOUT_H	R	GYRO_ZOUT_H							
22	34	GYRO_ZOUT_L	R	GYRO_ZOUT_L							
35	53	DMP_REG1	R/W	RESERVED1							
36	54	DMP_REG2	R/W	RESERVED2							
37	55	DMP_REG3	R/W	RESERVED3							
38	56	DMP_REG4	R/W	RESERVED4							
39	57	DMP_REG5	R/W	RESERVED5							
3A	58	FIFO_COUNTH	R	-	-	-	-	-	-	FIFO_COUNT_H	
3B	59	FIFO_COUNTL	R	FIFO_COUNT_L							
3C	60	FIFO_R	R	FIFO_DATA							
3D	61	USER_CTRL	R/W	DMP_EN	FIFO_EN	AUX_IF_EN	-	AUX_IF_RST	DMP_RST	FIFO_RST	GYRO_RST
3E	62	PWR_MGM	R/W	H_RESET	SLEEP	STBY_XG	STBY_YG	STBY_ZG	CLK_SEL		

10 Register Description

This section details each register within the InvenSense IMU-3000 gyroscope. Note that any bit that is not defined should be set to zero in order to be compatible with future InvenSense devices.

The register space allows single-byte reads and writes, as well as burst reads and writes. When performing burst reads or writes, the memory pointer will increment until either (1) reading or writing is terminated by the master, or (2) the memory pointer reaches registers 57 or 60.

10.1 Register 0 – Who Am I

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	ID						-

Description:
This register is used to verify the identity of the device.
Parameters:

ID Contains the I^2C address of the device, which can be changed by writing to this register.
0 This register bit must be set to 0 when writing to this register.

The Power-On-Reset value of Bit6: Bit1 is 110 100.

The Power-On-Reset value of Bit7 is 0.

10.2 Registers 12 to 17 – Gyro Offsets

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C	12	X_OFFS_H							
D	13	X_OFFS_L							
E	14	Y_OFFS_H							
F	15	Y_OFFS_L							
10	16	Z_OFFS_H							
11	17	Z_OFFS_L							

Description:
These registers are used to remove DC bias from the sensor outputs. The values in these registers are subtracted from the gyro sensor values before going into the sensor registers (see registers 29 to 34).

Parameters:
X_OFFS_H/L 16-bit offset (high and low bytes) of X gyro offset (2's complement)
Y_OFFS_H/L 16-bit offset (high and low bytes) of Y gyro offset (2's complement)
Z_OFFS_H/L 16-bit offset (high and low bytes) of Z gyro offset (2's complement)

10.3 Register 18 – FIFO Enable

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
12	18	TEMP_ OUT	GYRO_ XOUT	GYRO_ YOUT	GYRO_ ZOUT	AUX_ XOUT	AUX_ YOUT	AUX_ ZOUT	FIFO_ FOOTER	00h

Description:
This register determines what data goes into the IMU-3000 FIFO, which is a 512 byte First-In-First-Out buffer (see register 60). Sensor data is automatically placed into the FIFO after each ADC sampling period is complete. The ADC sample rate is controlled by register 21.

The order at which the data is put into the FIFO is from MSB to LSB, which means that it will match the order shown in the parameter detail below. Two bytes are used for each reading. For example, if Gyro X, Gyro Y, Gyro Z, and FIFO_FOOTER are configured to go into the FIFO, then each sample period the following 8 bytes would be inserted into the FIFO, as shown below:

Gyro X High byte	Gyro X Low byte	Gyro Y High byte	Gyro Y Low byte	Gyro Z High byte	Gyro Z Low byte	FIFO_FOOTER High byte	FIFO_FOOTER Low byte

Parameters:

TEMP_OUT	Setting this inserts the Temperature reading into FIFO
GYRO_XOUT	Setting this inserts the X Gyro reading into FIFO
GYRO_YOUT	Setting this inserts the Y Gyro reading into FIFO
GYRO_ZOUT	Setting this inserts the Z Gyro reading into FIFO
AUX_XOUT	Setting this inserts the X Accelerometer reading into FIFO
AUX_YOUT	Setting this inserts the Y Accelerometer reading into FIFO
AUX_ZOUT	Setting this inserts the Z Accelerometer reading into FIFO
FIFO_FOOTER	Last word (2 bytes) for FIFO read. Described in more detail in Section 60

10.4 Registers 19 – AUX (Accel) VDDIO

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
13	19	0	0	0	0	0	AUX_ VDDIO	0	0	00h

Description:
This register determines the I/O logic levels for the secondary I^2C bus clock and data lines (AUX_CL, AUX_DA). 1=VDD, 0=VLOGIC.

Parameters:

AUX_VDDIO	I/O logic levels for the secondary I^2C bus clock and data lines (AUX_CL, AUX_DA). 1=VDD, 0=VLOGIC.
0	Load zeros into Bits 0, 1, 3-7.

10.5 Register 20 – AUX (Accel) Slave Address

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
14	20	CLKOUTEN	AUX_ID							00h

Description:

This register contains the enable bit for the reference clock output and the 7-bit slave address of the external 3rd party accelerometer.

The CLKOUTEN bit is used to enable (1) or disable (0) the reference clock output at the CLKOUT pin.

AUX_ID, the 7-bit accelerometer slave address, is used to access the accelerometer so that its sensor reading can be automatically read during each sample period at the same time as the gyro sensors.

When reading the external accelerometer registers, the IMU-3000 takes over the secondary I^2C bus, as a master to the accel, performing a burst read of the sensor registers. For this interface to be active, the AUX_*IF_EN* flag in the User Control register (61) must be set (set to 1).

Whenever changing this register, the secondary accel interface must be reset with AUX_*IF_RST* to take effect. Refer to the User Control register (61).

Parameters:

CLKOUTEN The enable bit for the reference clock output that is provided at the CLKOUT pin. 1=clock output enabled; 0=clock output disabled.

AUX_ID Contains the I^2C address of the external accelerometer. The address can be changed by writing to this register.

10.6 Register 21 – Sample Rate Divider

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
15	21	SMPLRT_DIV								00h

Description:

This register determines the sample rate of the IMU-3000 gyros. The analog gyros are sampled internally at either 1kHz or 8kHz, determined by the *DLPF_CFG* setting (see register 22). This sampling is then filtered digitally and delivered into the sensor registers after the number of cycles determined by this register. The sample rate is given by the following formula:

$F_{sample} = F_{internal} / (divider+1)$, where $F_{internal}$ is either 1kHz or 8kHz

As an example, if the internal sampling is at 1kHz, then setting this register to 7 would give the following:

F_{sample} = 1kHz / (7 + 1) = 125Hz, or 8ms per sample

Parameters:

SMPLRT_DIV Sample rate divider: 0 to 255

10.7 Register 22 – DLPF, Full Scale

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
16	22	0	0	0	FS_SEL		DLPF_CFG			00h

Description:
This register configures parameters related to the sensor acquisition.

The *FS_SEL* parameter allows setting the full-scale range of the gyro sensors, as described in the table below.

FS_SEL

FS_SEL	Gyro Full-Scale Range
0	±250°/sec
1	±500°/sec
2	±1000°/sec
3	±2000°/sec

The *DLPF_CFG* parameter sets the digital low pass filter configuration. It also determines the internal analog sampling rate used by the device as shown in the table below.

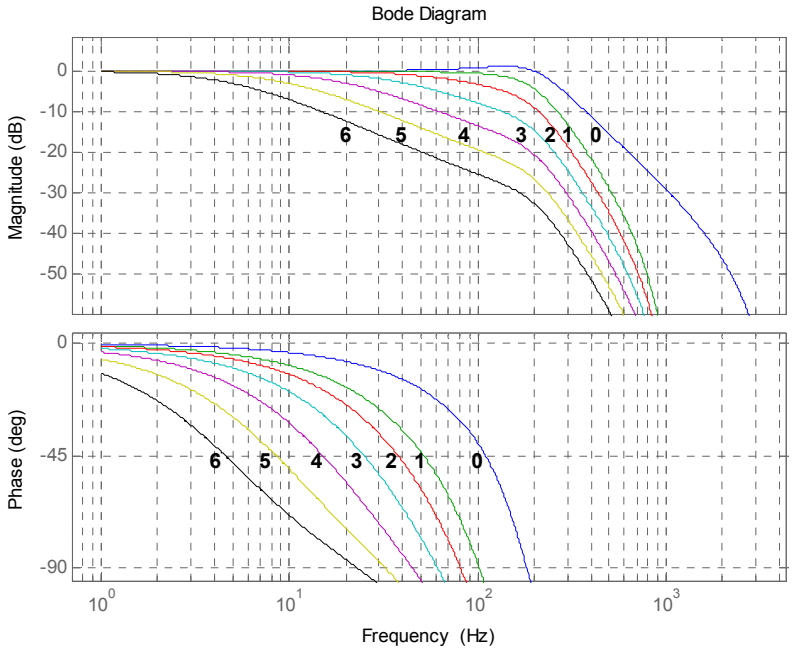
DLPF_CFG

DLPF_CFG	Low Pass Filter Bandwidth	Analog Sample Rate
0	256Hz	8kHz
1	188Hz	1kHz
2	98Hz	1kHz
3	42Hz	1kHz
4	20Hz	1kHz
5	10Hz	1kHz
6	5Hz	1kHz
7	Reserved	Reserved

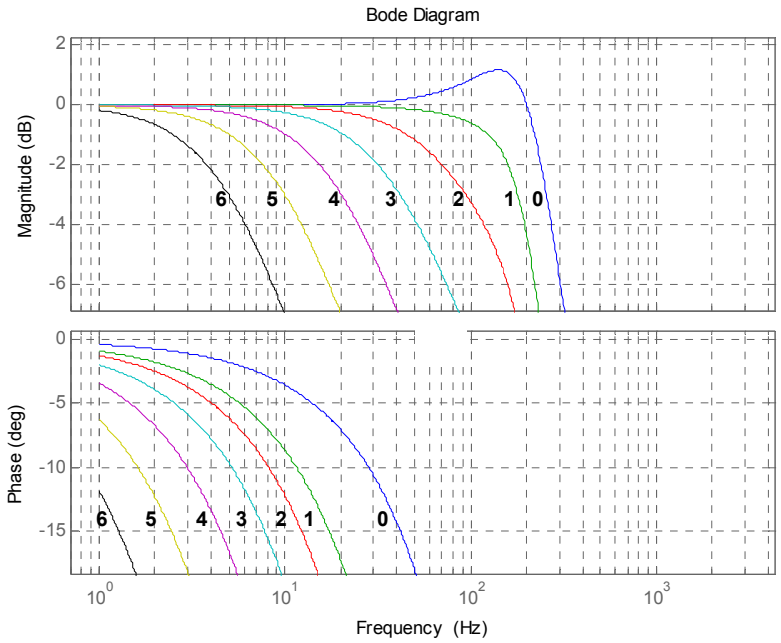
Parameters:

FS_SEL	Full scale selection for gyro sensor data
DLPF_CFG	Digital low pass filter configuration
0	Load zeros into Bits 5-7 of the DLPF, Full Scale register

DLPF Characteristics: The gain and phase responses of the digital low pass filter settings (*DLPF_CFG*) are shown below:



Gain and Phase vs. Digital Filter Setting



Gain and Phase vs. Digital Filter Setting, Showing Passband Details

10.8 Register 23 – Interrupt Configuration

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
17	23	ACTL	OPEN	LATCH_INT_EN	INT_ANYRD_2CLEAR	I2C_MST_ERR_EN	IMU_RDY_EN	DMP_DONE_EN	RAW_RDY_EN	00h

Description:

This register configures the interrupt operation of the IMU-3000. The interrupt output pin (INT) configuration can be set, the interrupt latching/clearing method can be set, and the triggers for the interrupt can be set. If LATCH_INT_EN = 1, the INT pin is held active until the interrupt status register is cleared.

Note that if the application requires reading every sample of data from the IMU-3000, it is best to enable the raw data ready interrupt (*RAW_RDY_EN*). This allows the application to know when new sample data is available.

Parameters:

ACTL	Logic level for INT output pin – 1=active low, 0=active high
OPEN	Drive type for INT output pin – 1=open drain, 0=push-pull
LATCH_INT_EN	Latch mode – 1=latch until interrupt is cleared, 0=50µs pulse
INT_ANYRD_2CLEAR	Interrupt status register clear method – 1=clear by reading any register, 0=clear by reading interrupt status register (26) only
I2C_MST_ERR_EN	Enable interrupt when accelerometer on secondary I^2C bus does not acknowledge IMU-3000
IMU_RDY_EN	Enable interrupt when device is ready (PLL ready after changing clock source)
DMP_DONE_EN	Enable interrupt when DMP is done (programmable functionality)
RAW_RDY_EN	Enable interrupt when data is available

10.9 Register 24 – AUX (Accel) Burst Read Address / Secondary I^2C Bus I/O Level

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
18	24	BURST_ADDR								00h

Description:

This register configures the burst-mode-read starting address for an accelerometer attached to the secondary I^2C bus of the IMU-3000, and determines the I/O logic levels of the secondary I^2C bus clock and data lines (AUX_CL, AUX_DA).

Parameters:

AUX_VDDIO	I/O logic levels for the secondary I^2C bus clock and data lines (AUX_CL, AUX_DA; 1=VDD, 0=VLOGIC)
BURST_ADDR	Burst-mode-read starting address for external accelerometer attached to secondary I^2C bus of the IMU-3000.

10.10 Register 26 – Interrupt Status

Type: Read only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
1A	26	FIFO_FULL	-	-	-	I2C_MST_ERR	IMU_RDY	DMP_DONE	RAW_DATA_RDY	00h

Description:

This register is used to determine the status of the IMU-3000 interrupt. Whenever one of the interrupt sources is triggered, the corresponding bit will be set. The polarity of the interrupt pin (active high/low) and the latch type (pulse or latch) has no affect on these status bits.

In normal use, the *RAW_DATA_RDY* interrupt is used to determine when new sensor data is available in either the sensor registers (27 to 34) or in the FIFO (60).

Interrupt Status bits get cleared as determined by INT_ANYRD_2CLEAR in the interrupt configuration register (23).

Parameters:

FIFO_FULL	FIFO has overflowed. Cleared when Register 26 is read and when *FIFO_RST* (register 61) is set.
I2C_MST_ERR	The IMU-3000 did not receive an acknowledge from the accelerometer on the secondary I^2C bus when the IMU-3000 was acting as a master
IMU_RDY	PLL ready
DMP_DONE	Digital Motion Processor (DMP) is done
RAW_DATA_RDY	Raw data or FIFO data is ready

10.11 Registers 27 to 34 – Sensor Registers

Type: Read only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value*
1B	27	TEMP_OUT_H								00h
1C	28	TEMP_OUT_L								00h
1D	29	GYRO_XOUT_H								00h
1E	30	GYRO_XOUT_L								00h
1F	31	GYRO_YOUT_H								00h
20	32	GYRO_YOUT_L								00h
21	33	GYRO_ZOUT_H								00h
22	34	GYRO_ZOUT_L								00h

*Default Value applies if sensor is disabled.

Description:

These registers contain the gyro and temperature sensor data for the IMU-3000. At any time, these values can be read from the device; however it is best to use the interrupt function to determine when new data is available.

If the FIFO is used, the contents of these registers are automatically copied into the FIFO at each sample period, and then this data can be read from the FIFO (register 60).

Before being placed into these registers, the sensor data are first manipulated by the full scale setting (register 22) and the offset settings (registers 12 to 17).

Parameters:

TEMP_OUT_H/L 16-bit temperature data (2's complement data format)
GYRO_XOUT_H/L 16-bit X gyro output data (2's complement data format)
GYRO_YOUT_H/L 16-bit Y gyro output data (2's complement data format)
GYRO_ZOUT_H/L 16-bit Z gyro output data (2's complement data format)

10.12 Registers 53 to 57 – DMP Registers

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
35	53	RESERVED1							
36	54	RESERVED2							
37	55	RESERVED3							
38	56	RESERVED4							
38	57	RESERVED5							

Description:

The data for these registers is included in a source code file supplied by InvenSense, and is used for the Digital Motion Processor (DMP) operation. This data is only necessary if the DMP is enabled using the User Control register (register 61).

Parameters:

RESERVED1 Reserved data1 for the DMP
RESERVED2 Reserved data2 for the DMP
RESERVED3 Reserved data3 for the DMP
RESERVED4 Reserved data4 for the DMP
RESERVED5 Reserved data5 for the DMP

10.13 Registers 58 to 59 – FIFO Count

Type: Read only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
3A	58	-	-	-	-	-	-	FIFO_COUNT_H		00h
3B	59	FIFO_COUNT_L								00h

Description:

These registers indicate how many bytes of valid data are contained in the FIFO. The FIFO can contain up to 512 bytes of data

If the FIFO gets filled up completely, the length will read 512. In this state, the IMU-3000 continues to put new sensor data into the FIFO, thus overwriting old FIFO data. Note, however, that the alignment of sensor data can change in this overflow condition. InvenSense recommends resetting the FIFO if an overflow condition occurs (use register 61), which will clear out the FIFO.

Parameters:

FIFO_COUNT_H/L Number of bytes currently in FIFO

10.14 Register 60 – FIFO Data

Type: Read only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
3C	60	FIFO_DATA								00h

Parameters:
FIFO_DATA Contains the FIFO data

Description:
This is the output register of the FIFO. Each read of this register gets the oldest contents of the IMU-3000 FIFO buffer; thus the data is read out in the same order that the IMU-3000 put the data in. If the FIFO operation is enabled, the IMU-3000 puts new data into the FIFO at each sample interval. The data that goes in is determined by the FIFO enable register (18).

A burst read or write is required for reading or writing *multiple* bytes to or from this register, since any read or write on this register causes an auto increment and a prefetch to occur.

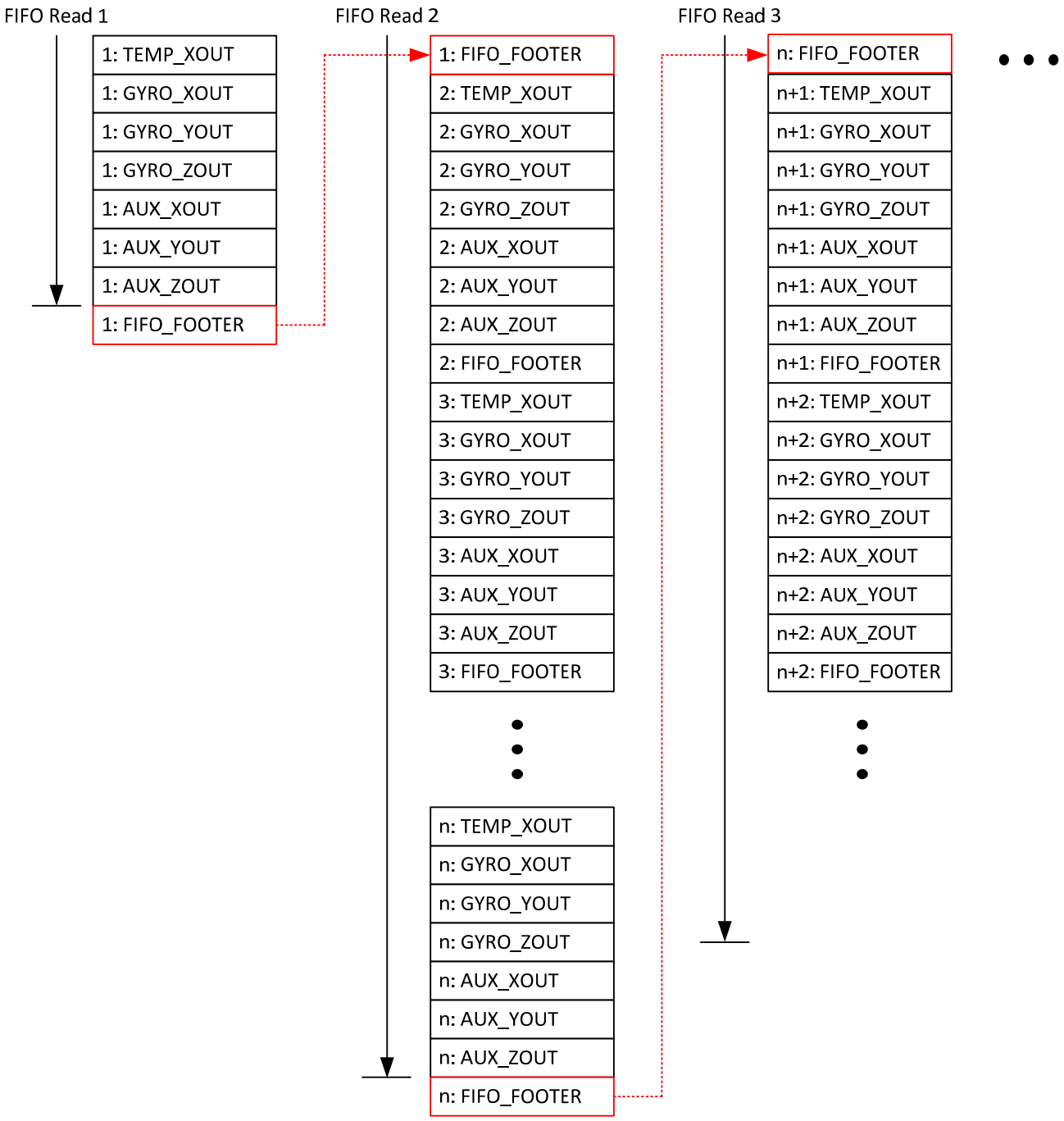
Proper operation of the FIFO requires that at least one word (2 bytes) of data be left in the FIFO during any read operation. To implement this, it is recommended that one extra two byte word (FIFO_FOOTER) be added to the end of the FIFO data so that all desired data can be read at each cycle, leaving the extra word remaining in the FIFO. This extra word will be read out (first) during the next read operation on the FIFO.
Data is read into the FIFO in the following order:

TEMP_OUT	Temperature high and low bytes (2 bytes)
GYRO_XOUT	X Gyro high and low bytes (2 bytes)
GYRO_YOUT	Y Gyro high and low bytes (2 bytes)
GYRO_ZOUT	Z Gyro high and low bytes (2 bytes)
AUX_XOUT	X Accelerometer high and low bytes (2 bytes)
AUX_YOUT	Y Accelerometer high and low bytes (2 bytes)
AUX_ZOUT	Z Accelerometer high and low bytes (2 bytes)
FIFO_FOOTER	*Last word for FIFO read (2 bytes)*

For example, if it is desired to obtain temperature, gyro, and accelerometer data from the FIFO, then one should also add FIFO_FOOTER into the FIFO enable register (18) in addition to the desired data. As shown in the figure below, the first time data is written to the FIFO, the FIFO will contain: *TEMP_OUT, GYRO_XOUT, GYRO_YOUT, GYRO_ZOUT, AUX_XOUT, AUX_YOUT, AUX_ZOUT,* and *FIFO_FOOTER*. The first FIFO read will read all but the *FIFO_FOOTER* data, which will be read in the 2nd FIFO read. In the 2nd FIFO read, the *FIFO_FOOTER* data that was left over from the previous read is read out first, followed by all but the last *FIFO_FOOTER* data in the FIFO. This pattern of reading is continued, as shown in the figure.

Note that the first FIFO read is similar to the subsequent reads in that one word of data is always left in the FIFO. It differs, though, in that the in subsequent reads the leftover data from the previous read is read first; however, for the first read there is no leftover data from a previous read.

If the FIFO is allowed to overflow, it operates as a circular buffer in which at any time it contains the most recent 512 bytes. Recommended operation in this mode is to disable data going into the FIFO prior to reading the FIFO to avoid pointer conflicts. After halting the FIFO input, the 512 bytes in the FIFO should be read out in a single burst read. The first byte read will not be valid.



Reading from the FIFO

(Note that AUX_XOUT, AUX_YOUT, and AUX_ZOUT are the X, Y, and Z accelerometer outputs, respectively.)

10.15 Register 61 – User Control

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
3D	61	DMP_EN	FIFO_EN	AUX_IF_EN	-	AUX_IF_RST	DMP_RST	FIFO_RST	GYRO_RST	00h

Description:

This register is used to enable various modes on the IMU-3000, as well as reset these functions.

For each of the functions that can be enabled, the function should be reset at the same time to assure it works properly. Note that the reset bits in the register are automatically cleared after the function is reset.

For example, to enable the FIFO set both the *FIFO_EN* and the *FIFO_RST* bits. This will start the FIFO storage on the next sample period.

As an additional example, for an external processor to communicate directly to the external accelerometer (i.e. have the secondary I^2C bus be directly connected to the primary I^2C bus), the AUX*_IF_EN* bit should be cleared and the AUX*_IF_RST* bit should be set. This will allow the I^2C bus to pass through the IMU-3000 and allow the processor to control the accelerometer device (as well as the IMU). Pass through mode is useful for allowing the processor to configure the accelerometer, since the IMU-3000 can perform burst reads on the accelerometer, but is not set up to configure the device.

Parameters:

DMP_EN	Enable Digital Motion Processor (DMP)
FIFO_EN	Enable FIFO operation for sensor data
AUX_IF_EN	Enable IMU as master to accelerometer interface via secondary I^2C (clear bit to configure primary I^2C bus to pass through directly to the secondary I^2C bus)
AUX_IF_RST	Reset secondary accelerometer interface function; set this whenever changing AUX*_IF_EN*
DMP_RST	Reset DMP function; set this whenever changing *DMP_EN*
FIFO_RST	Reset FIFO function; set this to clear FIFO or when changing *FIFO_EN*
GYRO_RST	Reset gyro analog and digital functions

10.16 Register 62 – Power Management

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
3E	62	H_RESET	SLEEP	STBY_XG	STBY_YG	STBY_ZG	CLK_SEL			00h

Description:

This register is used to manage the power control, select the clock source, and to issue a master reset to the device.

H_RESET is used to reset the device and set the internal registers to the power-up default settings.

STBY_XG, STBY_YG, and *STBY_ZG* are used to place the gyros into a standby or active mode (1=standby; 0=normal operating mode).

Setting the *SLEEP* bit in the register puts the device into a low power sleep mode. In this mode, only the serial interface and internal registers remain active, allowing for a very low standby current. Clearing this bit puts the device back into normal mode. The individual standby selections for each of the gyros should be used if any of them are not used by the application.

The *CLK_SEL* setting determines the device clock source as follows:

CLK_SEL

CLK_SEL	Clock Source
0	Internal oscillator
1	PLL with X Gyro reference
2	PLL with Y Gyro reference
3	PLL with Z Gyro reference
4	PLL with external 32.768kHz reference
5	PLL with external 19.2MHz reference
6	Reserved
7	Stop clock and synchronous reset clock state

On power up, the IMU-3000 defaults to the internal oscillator. It is highly recommended that the device is configured to use one of the gyros (or an external clock) as the clock reference, due to the improved stability.

Parameters:

H_RESET	Reset device and internal registers to the power-up-default settings
SLEEP	Enable low power sleep mode
STBY_XG	Put gyro X in standby mode (1=standby, 0=normal)
STBY_YG	Put gyro Y in standby mode (1=standby, 0=normal)
STBY_ZG	Put gyro Z in standby mode (1=standby, 0=normal)
CLK_SEL	Select device clock source

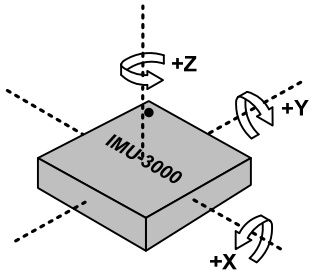
11 Assembly

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in Quad Flat No leads package (QFN) surface mount integrated circuits. The following six best practices will ensure higher quality in assembly.

1. Do not leave parts out of the original moisture-sealed bags for more than 48 hours before assembly
2. Do not solder the center pad
3. Do not place large insertion components, such as buttons, switches, connectors, or shielding boxes at a distance of less than 6 mm from the MEMS gyro
4. Do use Electrostatic Discharge (ESD) protection at or better than 200V, preferably 150V, to prevent Machine Model (MM) type ESD damage
5. Do use ESD protection measures to ensure that personnel prevent Human Body Model (HBM) type ESD damage
6. Do not mechanically impact or shock the package in any of the production processes

11.1 Orientation

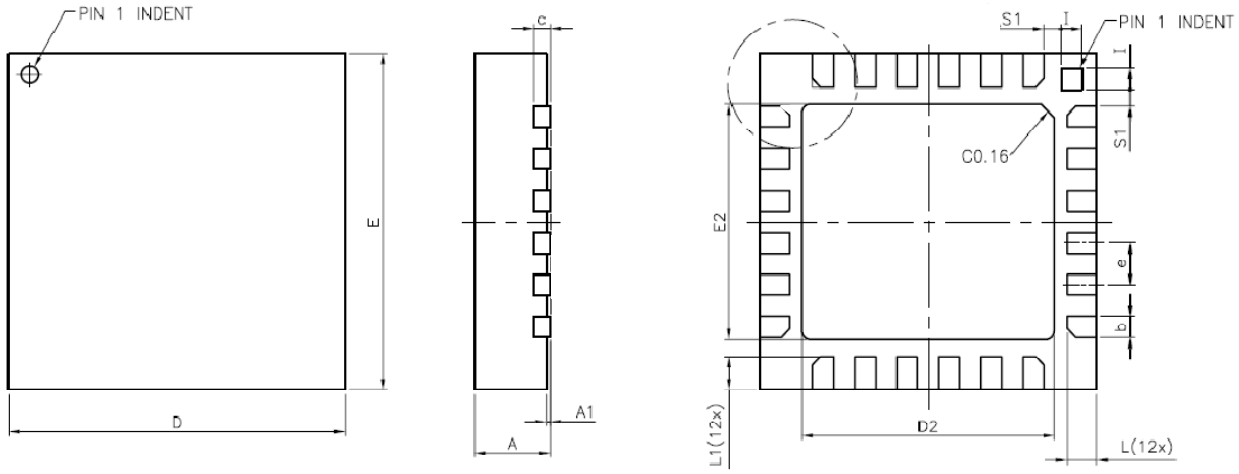
The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation.

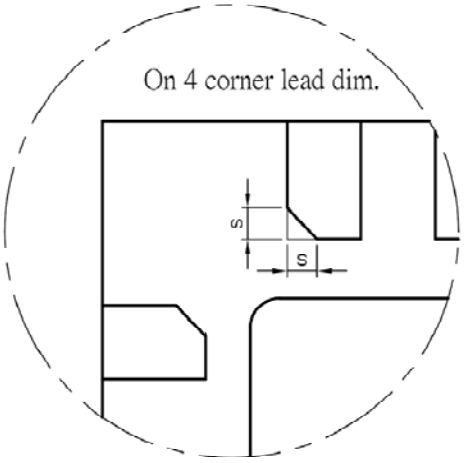


Orientation of Axes of Sensitivity and Polarity of Rotation

11.2 PCB Layout Guidelines

11.2.1 Package Dimensions





NOTE:
1.THE TERMINAL #1 IDENTIFIER IS A LASER MARKED FEATURE

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	——	0.20 REF.	——
D	3.90	4.00	4.10
D2	2.95	3.00	3.05
E	3.90	4.00	4.10
E2	2.75	2.80	2.85
e	——	0.50	——
L	0.30	0.35	0.40
L1	0.35	0.40	0.45
I	0.20	0.25	0.30
s	0.05	——	0.15
S1	0.15	0.20	0.25

11.2.2 PCB Design Guidelines

InvenSense MEMS Gyros sense rate of rotation. In addition, gyroscopes sense mechanical stress coming from the PCB. This PCB stress is minimized with simple design rules:

1. Component Placement – Testing indicates that there are no specific design considerations other than generally accepted industry design practices for component placement near the IMU-3000 gyroscope to prevent noise coupling and thermo-mechanical stress.
2. The area below the MEMS gyro (on the same side of the board) must be defined as a keep-out area. It is strongly recommended to not place any structure in top metal layer underneath the keep-out area.
3. Traces connected to pads should be as much symmetric as possible. Symmetry and balance for pad connection will help component self alignment and will lead to better control of solder paste reduction after reflow.
4. Testing indicates that 3-Volt peak-to-peak signals run under the gyro package or directly on top of the package of frequencies from DC to 1MHz do not affect the operation of the MEMS gyro. However, routing traces or vias under the MEMS gyro package such that they run under the exposed die pad is prohibited.
5. To achieve best performance over temperature and to prevent thermo-mechanical package stress, do not place large insertion components like buttons, connectors, or shielding boxes at a distance of less than 6 mm from the MEMS gyro.

11.2.3 Exposed Die Pad Precautions

The IMU-3000 has very low active and standby current consumption. The exposed die pad is not required for heat sinking, and should not be soldered to the PCB since soldering to it contributes to performance changes due to package thermo-mechanical stress.

11.2.4 Gyro Removal from PCB

Never apply high mechanical force while removing MEMS gyros from PCB. Otherwise, the QFN package leads can be removed and failure analysis of the gyro unit will be impossible. Tweezers are practical.
Do not apply a pulling force upward. Instead apply a gentle force sideward while heating. When sufficient heat has been applied, the unit will start to slide sideways and can now be pulled gently upwards with the tweezers.
In any case, mechanical or thermo-mechanical overstress during manual handling and soldering, (especially contact between the soldering iron or hot air gun and the package) has to be avoided.
If safe removal of the suspected component is not possible or deemed too risky, send the whole PCB or the part of the PCB containing the defective component back to InvenSense. If requested, we will return the PCB after we have removed the gyro.

11.3 Trace Routing

Testing indicates that 3-Volt peak-to-peak signals run under the gyro package or directly on top of the package of frequencies from DC to 1MHz do not affect the operation of the MEMS gyro. However, routing traces or vias under the MEMS gyro package such that they run under the exposed die pad is prohibited.

11.4 Soldering Exposed Die Pad

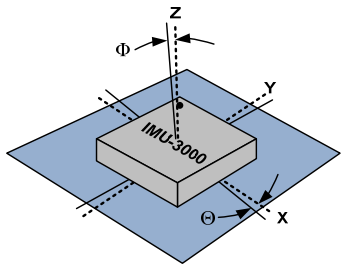
The IMU-3000 has very low active and standby current consumption. The exposed die pad is not required for heat sinking, and should not be soldered to the PCB since soldering to it contributes to performance changes due to package thermo-mechanical stress.

11.5 Component Placement

Do not place large insertion components such as keyboard or similar buttons, connectors, or shielding boxes at a distance of less than 6 mm from the MEMS gyro. Maintain generally accepted industry design practices for component placement near the IMU-3000 to prevent noise coupling and thermo-mechanical stress.

11.6 PCB Mounting and Cross-Axis Sensitivity

Orientation errors of the gyroscope mounted to the printed circuit board can cause cross-axis sensitivity in which one gyro responds to rotation about another axis, for example, the X-axis gyroscope responding to rotation about the Y or Z axes. The orientation mounting errors are illustrated in the figure below.



Package Gyro Axes (·····) Relative to PCB Axes (——) with Orientation Errors (Θ and Φ)

The table below shows the cross-axis sensitivity as a percentage of the specified gyroscope's sensitivity for a given orientation error.

Cross-Axis Sensitivity vs. Orientation Error

Orientation Error (θ or Φ)	Cross-Axis Sensitivity (sinθ or sinΦ)
0º	0%
0.5º	0.87%
1º	1.75%

The specification for cross-axis sensitivity in Section 3 includes the effect of the die orientation error with respect to the package.

11.7 MEMS Handling Instructions

MEMS (Micro Electro-Mechanical Systems) are a time-proven, robust technology used in hundreds of millions of consumer, automotive and industrial products. MEMS devices consist of microscopic moving mechanical structures. They differ from conventional IC products even though they can be found in similar packages. Therefore, MEMS devices require different handling precautions than conventional ICs prior to mounting onto printed circuit boards (PCBs).

The IMU-3000 gyroscope has a shock tolerance of 10,000*g*. InvenSense packages its gyroscopes as it deems proper for protection against normal handling and shipping. It recommends the following handling precautions to prevent potential damage.

- Individually packaged or trays of gyroscopes should not be dropped onto hard surfaces. Components placed in trays could be subject to *g*-forces in excess of 10,000*g* if dropped.
- Printed circuit boards that incorporate mounted gyroscopes should not be separated by manually snapping apart. This could also create *g*-forces in excess of 10,000*g.*

11.8 ESD Considerations

Establish and use ESD-safe handling precautions when unpacking and handling ESD-sensitive devices.

- The Tape-and-Reel moisture-sealed bag is an ESD approved barrier. The best practice is to keep the units in the original moisture sealed bags until ready for assembly.
- Restrict all device handling to ESD protected work areas that measure less than 200V static charge, or better, to less than 150V. Ensure that all workstations are properly grounded.
- Store ESD sensitive devices in ESD safe containers until ready for use.
- Ensure that personnel are properly grounded to prevent ESD.

11.9 Gyroscope Surface Mount Guidelines

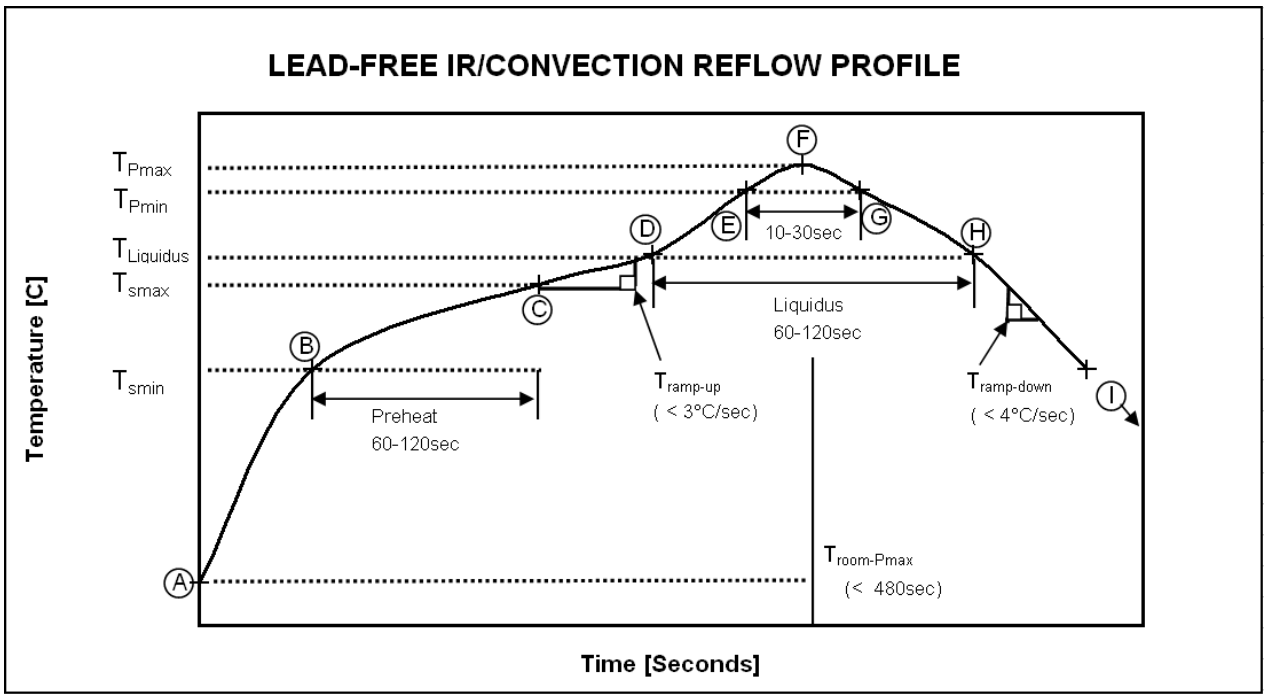
Any material used in the surface mount assembly process of the MEMS gyroscope should be free of restricted RoHS elements or compounds. Pb-free solders should be used for assembly.

In order to assure gyroscope performance, several industry standard guidelines need to be considered for surface mounting. These guidelines are for both printed circuit board (PCB) design and surface mount assembly and are available from packaging and assembly houses.

When using MEMS gyroscope components in plastic packages, package stress due to PCB mounting and assembly could affect the output offset and its value over a wide range of temperatures. This is caused by the mismatch between the Coefficient Temperature Expansion (CTE) of the package material and the PCB. Care must be taken to avoid package stress due to mounting.

11.10 Reflow Specification

The approved solder reflow curve shown in the figure below conforms to IPC/JEDEC J-STD-020D.01 (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) with a maximum peak temperature (Tc = 260°C). This is specified for component-supplier reliability qualification testing using lead-free solder for package thicknesses less than 1.6 mm. The reliability qualification pre-conditioning used by InvenSense incorporates three of these conforming reflow cycles. All temperatures refer to the topside of the QFN package, as measured on the package body surface. Customer solder-reflow processes should use the solder manufacturer's recommendations, making sure to never exceed the constraints listed in the table and figure below, as these represent the maximum tolerable ratings for the device. For optimum results, production solder reflow processes should use lower temperatures, reduced exposure times to high temperatures, and lower ramp-up and ramp-down rates than those listed below.



Approved IR/Convection Solder Reflow Curve

Temperature Set Points for IR / Convection Reflow Corresponding to Figure Above

Step	Setting	CONSTRAINTS		
		Temp (°C)	Time (sec)	Rate (°C/sec)
A	T_{room}	25		
B	T_{Smin}	150		
C	T_{Smax}	200	$60 < t_{BC} < 120$	
D	$T_{Liquidus}$	217		$r_{(TLiquidus-TPmax)} < 3$
E	T_{Pmin} [< TPmax-5°C, 250°C]	255		$r_{(TLiquidus-TPmax)} < 3$
F	T_{Pmax} [< TPmax, 260°C]	260	$t_{AF} < 480$	$r_{(TLiquidus-TPmax)} < 3$
G	T_{Pmin} [< TPmax-5°C, 250°C]	255	$t_{EG} < 30$	$r_{(TPmax-TLiquidus)} < 4$
H	$T_{Liquidus}$	217	$60 < t_{DH} < 120$	
I	T_{room}	25		

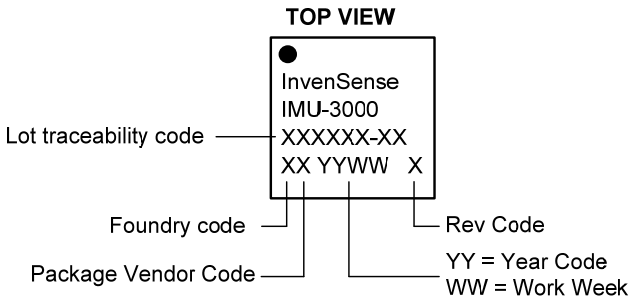
11.11 Storage Specifications

The storage specification of the IMU-3000 conforms to IPC/JEDEC J-STD-020C Moisture Sensitivity Level (MSL) 3.

Storage Specifications for IMU-3000

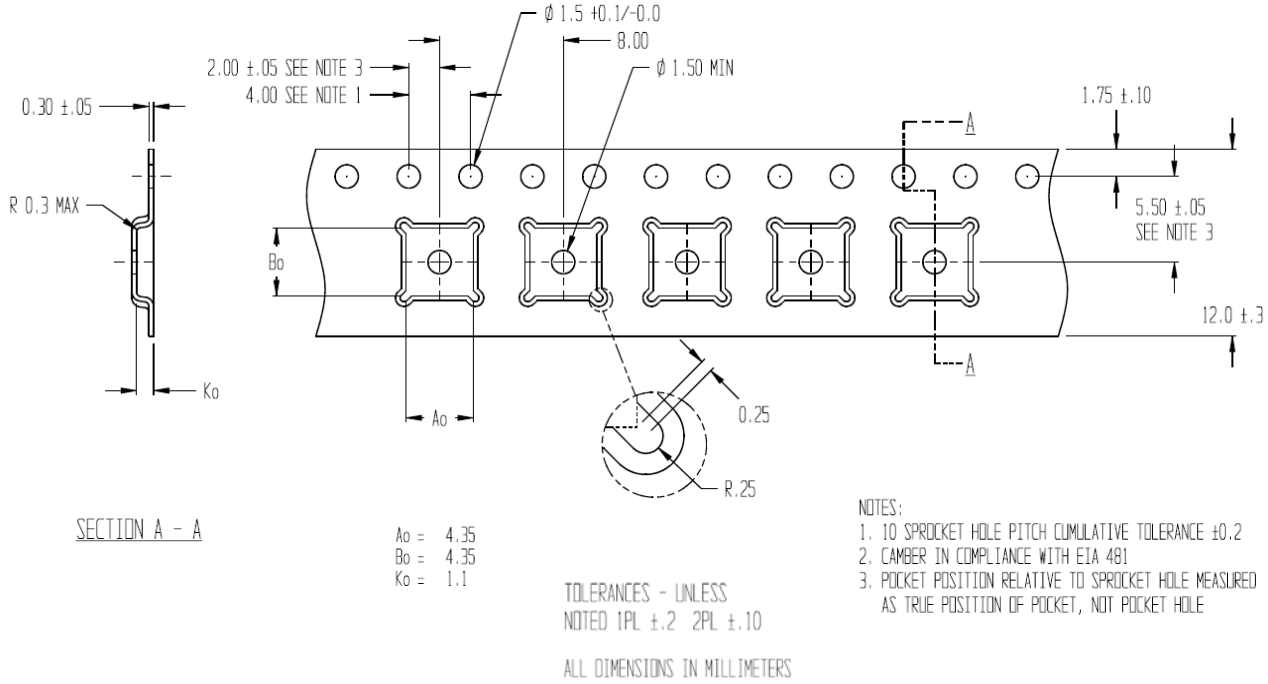
Calculated shelf-life in moisture-sealed bag	12 months -- Storage conditions: <40°C and <90% RH
After opening moisture-sealed bag	168 hours -- Storage conditions: ambient ≤30°C at 60% RH

11.12 Package Marking Specification

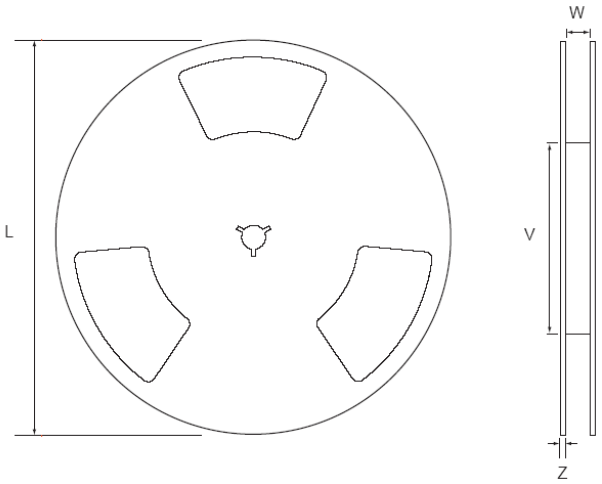


Package Marking Specification

11.13 Tape & Reel Specification



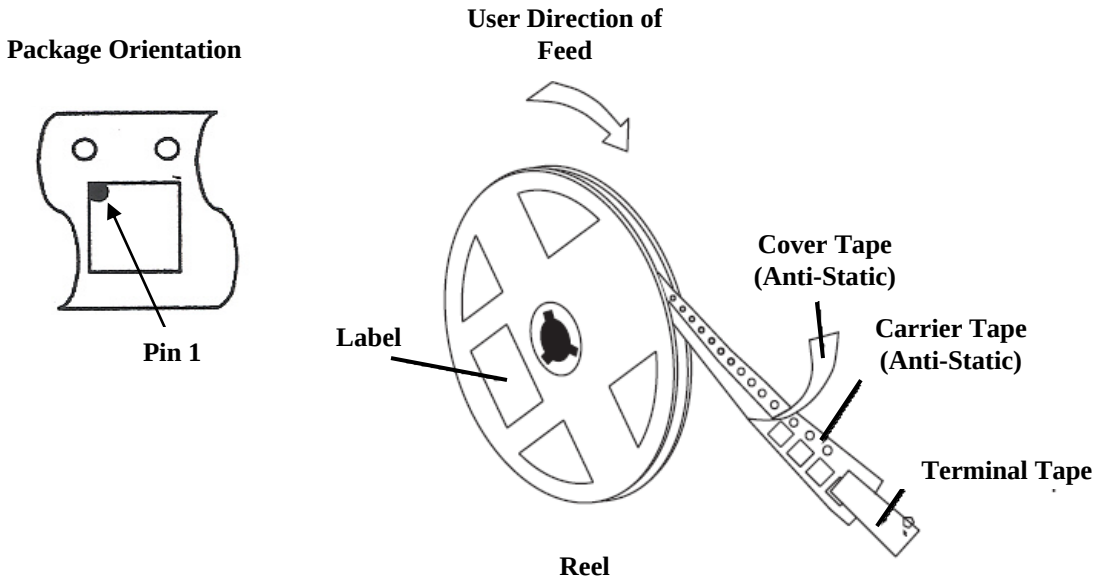
Tape Dimensions



Reel Outline Drawing

Reel Dimensions and Package Size

PACKAGE SIZE	REEL (mm)			
	L	V	W	Z
4x4	330	100	13.2	2.2

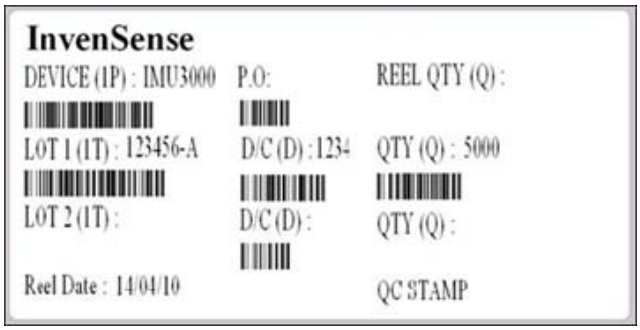


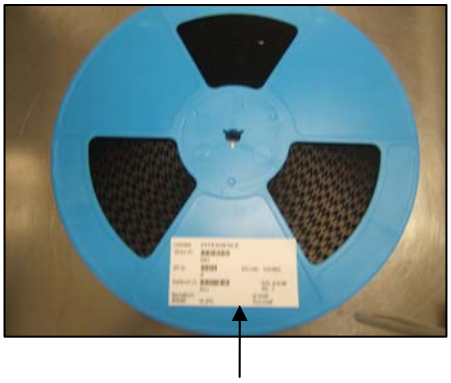
Tape and Reel Specification

Reel Specifications

Quantity Per Reel	5,000
Reels per Box	1
Boxes Per Carton (max)	3
Pieces per Carton (max)	15,000

11.14 Label





Location of Label

11.15 Packaging

Moisture Barrier Bag With Labels

Moisture-Sensitive Caution Label

Reel in Box

Box with Tape & Reel Label

12 Reliability

12.1 Qualification Test Policy

InvenSense's products complete a Qualification Test Plan before being released to production. The Qualification Test Plan follows the JEDEC 47D Standards, "Stress-Test-Driven Qualification of Integrated Circuits," with the individual tests described below.

12.2 Qualification Test Plan

Accelerated Life Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
High Temperature Operating Life (HTOL/LFR)	JEDEC JESD22-A108C, Dynamic, 3.63V biased, Tj>125°C [read-points 168, 500, 1000 hours]	3	77	(0/1)
Steady-State Temperature Humidity Bias Life (1)	JEDEC JESD22-A101C, 85°C/85%RH [read-points 168, 500 hours], Information Only 1000 hours]	3	77	(0/1)
High Temperature Storage Life	JEDEC JESD22-A103C, Cond. A, 125°C Non-Bias Bake [read-points 168, 500, 1000 hours]	3	77	(0/1)

Device Component Level Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
ESD-HBM	JEDEC JESD22-A114F, Class 2 (1.5KV)	1	3	(0/1)
ESD-MM	JEDEC JESD22-A115-A, Class B (200V)	1	3	(0/1)
Latch Up	JEDEC JESD78B Level 2, 125C, ±100mA	1	6	(0/1)
Mechanical Shock	JEDEC JESD22-B104C, Mil-Std-883, method 2002, Cond. D, 10,000*g's*, 0.3ms, ±X,Y,Z – 6 directions, 5 times/direction	3	5	(0/1)
Vibration	JEDEC JESD22-B103B, Variable Frequency (random), Cond. B, 5-500Hz, X,Y,Z – 4 times/direction	3	5	(0/1)
Temperature Cycling (1)	JEDEC JESD22-A104D Condition N, -40°C to +85°C, Soak Mode 2, 100 cycles	3	77	(0/1)

Board Level Tests

TEST	Method/Condition/	Lot Quantity	Sample / Lot	Acc / Reject Criteria
Board Mechanical Shock	JEDEC JESD22-B104C,Mil-Std-883, method 2002, Cond. D, 10,000*g's*, 0.3ms, +-X,Y,Z – 6 directions, 5 times/direction	1	5	(0/1)
Board T/C	JEDEC JESD22-A104D Condition N, -40°C to +85°C, Soak Mode 2, 100 cycles	1	40	(0/1)

(1) – Tests are preceded by MSL3 Preconditioning in accordance with JEDEC JESD22-A113F