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FDZ661PZ

December 2011

P-Channel 1.5 V Specified PowerTrench[®] Thin WL-CSP MOSFET -20 V, -2.6 A, 140 m Ω

Features

- Max $r_{DS(on)}$ = 140 m Ω at V_{GS} = -4.5 V, I_D = -2 A
- Max $r_{DS(on)}$ = 182 m Ω at V_{GS} = -2.5 V, I_D = -1.5 A
- Max r_{DS(on)} = 231 mΩ at V_{GS} = -1.8 V, I_D = -1 A
- Max r_{DS(on)} = 315 mΩ at V_{GS} = -1.5 V, I_D = -1 A
- Occupies only 0.64 mm² of PCB area. Less than 16% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.4 mm height when mounted to PCB
- HBM ESD protection level > 2 kV (Note3)
- RoHS Compliant

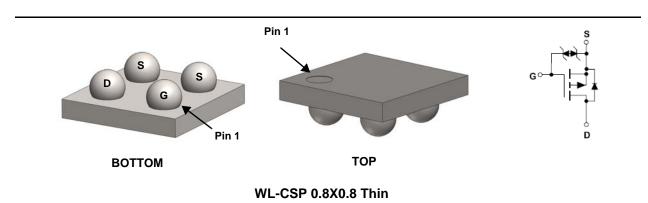


General Description

Designed on Fairchild's advanced 1.5 V PowerTrench[®] process with state of the art "fine pitch" Thin WLCSP packaging process, the FDZ661PZ minimizes both PCB space and $r_{DS(on)}$. This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile (0.4 mm) and small (0.8x0.8 mm²) packaging, low gate charge, and low $r_{DS(on)}$.

Applications

- Battery management
- Load switch
- Battery protection



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Para	meter		Ratings	Units
V _{DS}	Drain to Source Voltage			-20	V
V _{GS}	Gate to Source Voltage			±8	V
I _D	-Continuous	T _A = 25 °C	(Note 1a)	-2.6	•
	-Pulsed			-10	— A
P _D	Power Dissipation	T _A = 25 °C	(Note 1a)	1.3	14/
	Power Dissipation	T _A = 25 °C	(Note 1b)	0.4	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	93	°C/W
$R_{ extsf{ heta}JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	311	C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
EH	FDZ661PZ	WL-CSP 0.8X0.8 Thin	7 "	8 mm	5000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units	
Off Chara	acteristics						
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-20			V	
ΔBV_{DSS} ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = -250 \ \mu\text{A}$, referenced to 25 °C		-13		mV/°C	
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 V, V_{GS} = 0 V$			-1	μΑ	
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$			±6	μΑ	
On Chara	octeristics						
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \ \mu A$	-0.3	-0.7	-1.2	V	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \ \mu$ A, referenced to 25 °C		2.5		mV/°C	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -2 \text{ A}$		108	140	mΩ	
		V _{GS} = -2.5 V, I _D = -1.5 A		129	182		
		$V_{GS} = -1.8 \text{ V}, I_D = -1 \text{ A}$		159	231		
		$V_{GS} = -1.5 \text{ V}, I_D = -1 \text{ A}$		201	315		
		V_{GS} = -4.5 V, I _D = -2 A, T _J =125°C		143	204		
9fs	Forward Transconductance	$V_{DD} = -5 V, I_D = -2 A$		7.8		S	
Dynamic	Characteristics						
C _{iss}	Input Capacitance			416	555	pF	
C _{oss}	Output Capacitance	──V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz		61	80	pF	
C _{rss}	Reverse Transfer Capacitance			53	70	pF	
	g Characteristics						
t _{d(on)}	Turn-On Delay Time			4.9	10	ns	
t _r	Rise Time	V _{DD} = -10 V, I _D = -2.5 A,		6.3	13	ns	
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = -4.5 \text{ V}, \text{ R}_{GEN} = 6 \Omega$		68	108	ns	
t _f	Fall Time			33	52	ns	
Q _g	Total Gate Charge			6.3	8.8	nC	
Q _{gs}	Gate to Source Charge	$V_{GS} = -4.5 \text{ V}, \text{ V}_{DD} = -10 \text{ V},$ $I_{D} = -2.5 \text{ A}$		0.6		nC	
Q _{gd}	Gate to Drain "Miller" Charge			1.7		nC	

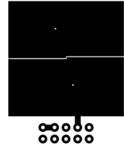
Notes:

t_{rr}

Q_{rr}

1. R_{BJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{BJC} is guaranteed by design while R_{BCA} is determined by the user's board design.

I_F = -2.5 A, di/dt = 100 A/μs



a. 93 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 311 °C/W when mounted on a minimum pad of 2 oz copper.

29

10

46

18

ns

nC

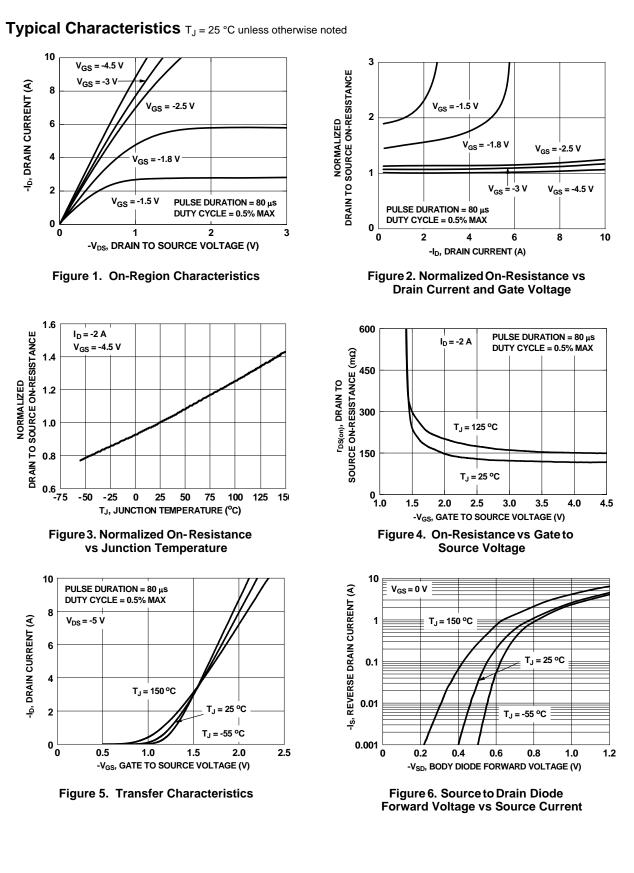
2. Pulse Test: Pulse Width < 300 $\mu s,$ Duty cycle < 2.0%.

Reverse Recovery Time

Reverse Recovery Charge

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

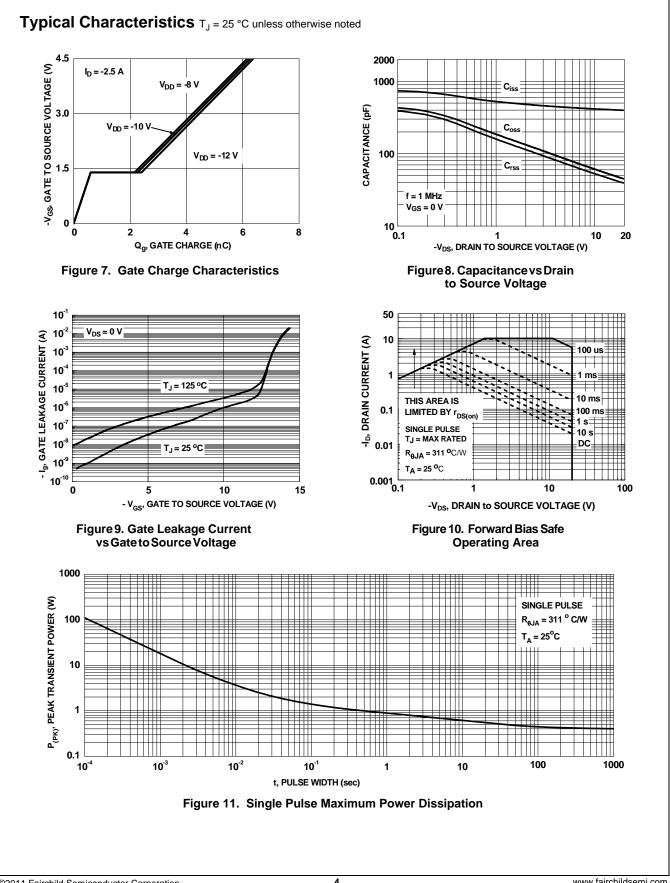
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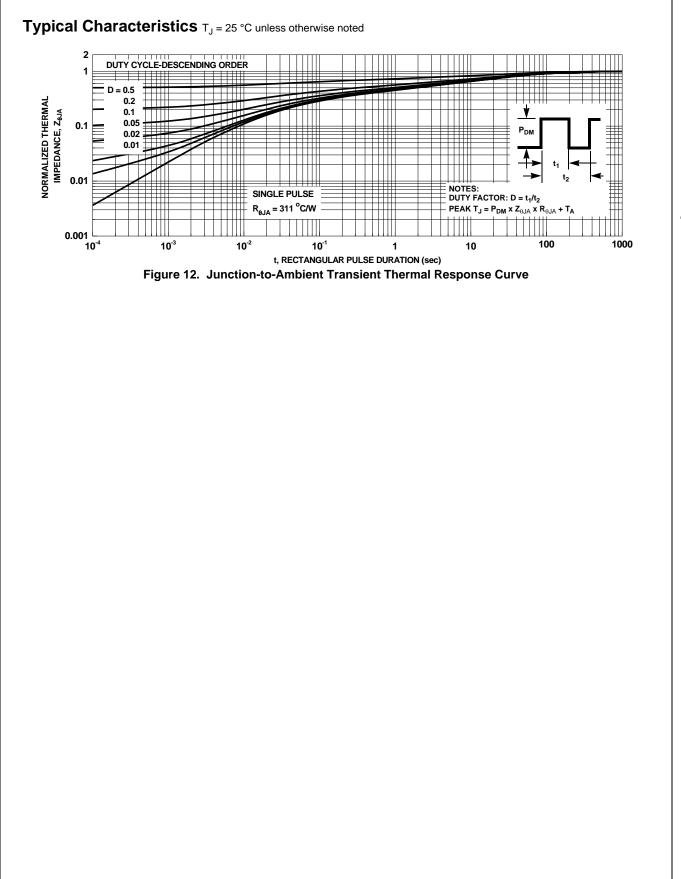
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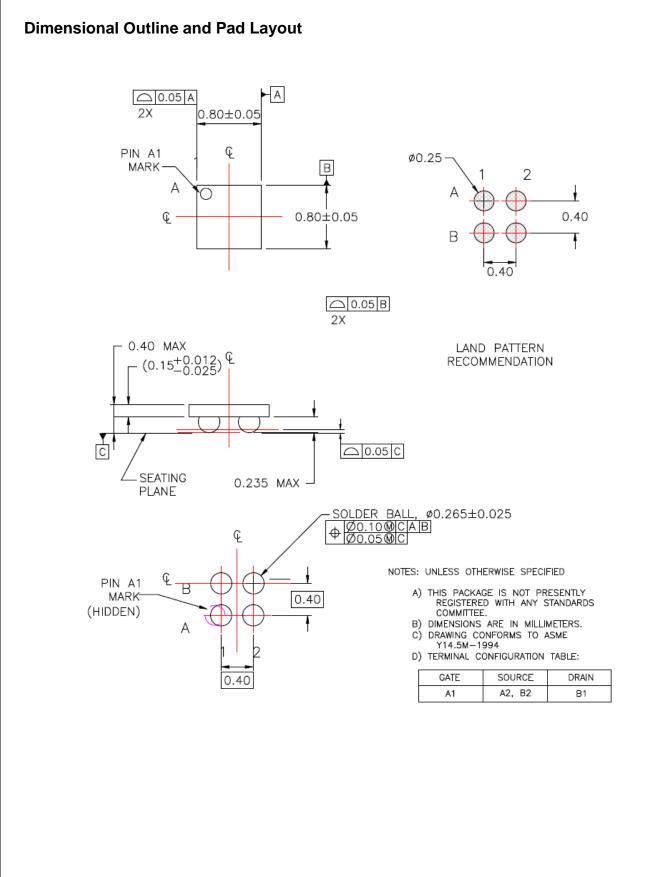
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